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NON DISSIPATIVE SOLAR ARRAY OPTIMUM CHARGE REGULATOR

FIRST QUARTERLY REPORT NAS5-9210

OCTOBER 1965

AEROSPACE GROUP

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

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ILLUSTRATIONS

1.0 SUMMARY OF EFFORT DURING THE FIRST QUARTER

This report summarizes a research of the field of optimum power transfer circuits which are capable of coupling the spacecraft solar array to a spacecraft type battery under the specified mission environmental conditions. Efficient use of all available power is necessary if the solar panel and radiator weights are to be kept to a minimum. Circuit efficiency is of key importance in the design of a reliable system as component reliability is a direct function of stress level. By maintaining efficient operation in the power transfer circuits, failure rates are greatly reduced and the probability of mission success is enhanced.

In the past, linear regulator circuits have been employed to couple power between the solar array and the battery. A linear amplifier is inherently limited in efficiency because of the minimum operating voltages for linear operation. Such considerations have led to the selection of a switching mode regulator as the means of power transfer. This circuit achieves high efficiency due to the fact that the main power transistor is either in the saturated condition or in the "open" condition. Therefore, the major power loss occurs during the time that the transistor is switching between these two states. These losses can be minimized by use of high speed transistors which are currently available.

Research in the area of optimum coupling and control techniques was performed in conjunction with the study of linear versus switching operation. Based on this study, an extremal seeking controller was found to be the best means by which optimum power transfer could be realized. This type of control is utilized in the Surveyor spacecraft battery charge regulator successfully. Under certain conditions, it allows the usage of almost 98 percent of the available solar array power. As a result of the study, a generalized design is presented which is based on a switching regulator with an extremal seeking controller.

In addition to the circuit study, research was performed to determine the types of battery systems that could be effectively utilized. Orbital conditions were derived and batteries were selected which would meet the given performance requirements. Battery control devices to permit sensing of optimum charge were investigated.

2.0 PROJECTION OF WORK TO BE ACCOMPLISHED

2.1 GENERAL SUMMARY

During the next three quarters, the application of the knowledge gained during the first reporting period will be applied to the two case studies defined in NASA document PC#636-38094 and summarized in table I. In addition, verification of the design will be determined experimentally and all additions or corrections to the design will be made as needed. The breadboard phase of the program will be completed with the integration of the breadboards to the battery.

For the Case I study, it is anticipated that the basic method and the transient response modification will be used. The basic method is described in detail in Section 4 of this report. The transient response modification should enable the OCR to track the changes in the solar array power with a minimum increase in hunting loss. In order to

	Solar Panel Characteristics				Battery Characteristics		
	Open Circuit Voltage at 30°C		Rated Power		Voltage Range		Probable Type
	Min.*	Nominal	Min.*	Nominal	Min.	Max.	
Case I	21 V	30 V	35 W	50 W	12 V	20 V	Silver Cadmium or Silver Zinc
Case II	-	50 V	-	250 W	25 V	40 V	Nickel-Cadmium

*Expected transient conditions, 10-20 millisecond rise and fall times

Table I. Summary of electrical characteristics.

track the solar array, the nominal hunting frequency will have to be approximately 500 to 1000 cps. This will force the switching frequency of the switching power transfer circuit to be around 10KC. However, it should still be feasible to achieve a 90 percent efficiency with the present state of the art devices.

For the Case II study, it is anticipated that the basic method plus the transient response and the hunting loss reduction modifications will be utilized. These modifications to the basic method will allow the OCR to follow the normal variations of the solar array and the battery. It will further reduce the hunting losses. The hunting frequency in this case will be around 50 to 100 cps, which will allow the switching power transfer circuit's frequency to be around 2KC. The low switching frequency plus the higher solar array and battery voltages should allow an efficiency 90 percent to be achieved.

2.2 PROJECTION OF WORK FOR THE FOLLOWING PERIOD.

2.2.1 Circuit Design

The circuit design for both case studies will be completed during this period. This includes the design tradeoffs of efficiency, weight, and reliability. The breadboarding during this phase will be primarily for circuit feasibility and analytical verification.

2.2.2 Breadboarding and Testing

After completion of the circuit design, the breadboard fabrication will be accomplished. The testing during this period will be primarily aimed at verifying whether or not each block is capable of properly performing its intended function. In addition, some testing of integrated blocks should be completed.

2.2.3 Solar Array Simulator

The majority of tests will require a solar array simulator for a primary power source. It will be necessary to design and fabricate a source that is suitable for the circuit development needs. These

features should include different curves having the same maximum power, a source that stores almost no energy, and the ability to be electronically varied with a signal generator. These features will allow the simulator to exhibit the characteristics of the spin stabilized solar array and to determine the circuit susceptability to noise signals.

2.2.4 Battery Investigation

1. Procure and initiate tests on selected nickel-cadmium, silver-cadmium and silver-zinc cells.
2. Conduct tests on battery packs using selected charge and discharge parameters at various temperatures
3. Study and determine characteristics of various sensor and charge control techniques as reflected in battery performance.

2.3 PROPOSED SCHEDULE

2.3.1 The following is a chronological schedule for the circuit design for the second quarter of this program.

a. Design and Fabricate a solar array simulator.
b. Complete the circuit design for both case studies.
c. Start the breadboard testing.

2.3.2 The following is a brief schedule for the last two quarters of the program for the circuit design.

a. Complete all breadboard testing, including noise susceptibility and generation tests.
b. Perform breadboard environmental tests
c. Perform breadboard integration tests with battery and simulated battery loads.
d. Prepare breadboards, simulator, and batteries for shipment.
e. Prepare monthly and quarterly reports
f. Prepare final report.

2.3.3 The following is a chronological schedule for the battery study for the second quarter of this program.

a. Procure cells of the nickel-cadmium, silver-cadmium, and silver-zinc types.
b. Perform tests on battery packs using selected charge and discharge parameters.
c. Study and determine characteristics of various sensor and charge control techniques.

2.3.4 The following is a brief schedule for the last two quarters of the program for the battery study.

a. Complete all testing started in 2.3.3.
b. Delivery suitable batteries to circuit design for integration tests.
c. Prepare monthly and quarterly reports.
d. Prepare final report.

3.0 REVIEW OF EXISTING CONTROL TECHNIQUES

In the past two basic techniques have been used to couple the power from the solar array to the battery. Both of these techniques had the disadvantage of being inefficient as well as not being able to utilize the maximum power available. These two linear techniques can be basically described as the series and shunt regulator approach to the problem.

3.1 SERIES REGULATOR

This technique utilizes a series transistor between the solar array and the battery, as shown in Figure 3-1. When the battery voltage is low, Q1 is turned full on and the battery is allowed to charge at the maximum current rate available from the solar panel at the battery voltage. This is very inefficient, however, since the power delivered to the battery is I_{pi} times V_{bat}, where I_{pi} is the current drawn from the solar array at P_1, as indicated in Figure 3-2. As seen in Figure 3-2, if a set of contant power hyperbole is superimposed on the solar array characteristics, the maximum power available occurs at P_2. Therefore, the difference in power between P_1 and P_2 is lost and cannot be utilized. This can be termed as system inefficiency for the power was available but not transferred to the system.

When the battery has charged to a preset maximum voltage, the inhibit circuit of Figure 3-1 takes over and begins to turn Q1 "off". This causes the operating point to move to P3 and the regulator allows

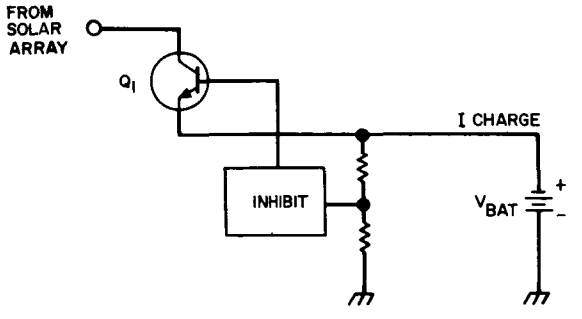

Figure 3-1. Series regulator schematic diagram.

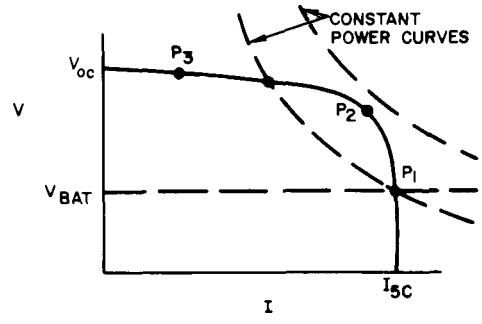

Figure 3-2. Typical solar array characteristics.

just enough current to flow to trickle charge the battery and maintain maximum charge.

3.2 SHUNT REGULATOR

This technique utilizes a parallel transistor across the solar array output as shown in Figure 3-3. When the battery voltage is low, Q1 is "off" and the operating point is P1 of Figure 3-2. When it reaches full charge, the operating point remains at P1 and Q1 begins to turn on which bypasses the current away from the battery. This system is even less efficient than the series technique because of the continuous power drain from the solar panel which must be dissipated.

3.3 WEIGHT VS EFFICIENCY

Since the two techniques previously described inefficiently couple power to the battery, then the solar array maximum power output

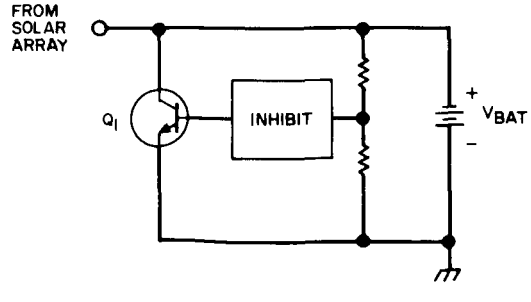

Figure 3-3. Shunt regulator schematic diagram.

would have to be increased by that inefficiency factor. This would be necessary to insure that the battery state of charge be maintained at the maximum required for system operation.

Another problem is that of heat transfer due to regulator dissipation. A radiator would be required to perform this function.

With unit emissivity and no solar loading, one square foot of radiator can transfer 57.3 watts to space and the associated weight at 141 lbs per square is 244 pounds per KW. This assumes a radiator temperature of 50°C. A typical solar panel has an associated weight of about 230 lbs/KW. Therefore for a 50 percent efficient system where it is required to deliver 50 watts to the battery, the associated weight increase would be 23.7 lbs. A plot of weight increase versus efficiency is seen in Figure 3-4.

3.4 SWITCHING REGULATOR

Because of the factors considered in the previous sections, the switching mode of operation with its inherently high efficiency was chosen as the heart of the power transfer scheme. Another factor in its favor, is the proven ability to match the solar panel characteristic to that of the battery and the ability to draw the maximum power available from the solar panel. This maximum power transfer is obtained

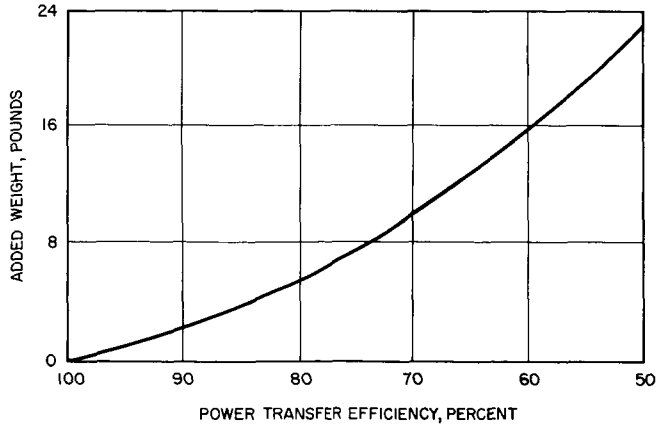

Figure 3-4. Weight tradeoff, OCR vs solar array power output.

by the fact that the regulator matches the battery voltage to the solar panel and makes it appear that this voltage is associated with point P2 of Figure 3-2.

The Surveyor optimum charge regulator operates in this manner. It transfers the maximum power from a 33 to 46 volt solar array into a 17 to 27.5 volt battery. The Surveyor OCR has a nominal efficiency of 85 percent at a solar array power of 90 watts. The circuit employs the self oscillating loop with a differentiating detector. The optimum charge regulator circuits weigh approximately 2.5 pounds and occupy approximately 90 cubic inches.

The operation of the OCR is identical to the basic method explained in Section 4. However, the modifications to the basic method were not conceived of at the time of the original design. The modifications should permit the efficiency to be improved by reducing the susceptibility compromises, by reducing the excursions of the oscillation about the maximum power point, and by changing the filter designs. By doing this a 90 percent efficiency becomes feasible.

3.5 REFERENCES

The following list summarizes some of the available texts and articles which treat the subjects of spacecraft power conversion systems and optimum control systems. These documents were used as background material for this study.

Further information on spacecraft power conversion systems may be found in the following article,

1. Astronautics and Aerospace Engineering, Static Power Conversion for Spacecraft - Koerner, May 1963.

Further information in the area of optimum control systems theory may be found in the following,

2. "Principles of Optimalizing Control Systems and Application to the Internal Combustion Engine," by C. S. Draper and Y. T. Li from The American Society of Mechanical Engineers.

3. "Synthesis of Optimum Control Systems," by Chang from McGraw Hill Series in Control Engineering.
4. Handbook of Automation Computation and Control, Grabbe, Ramo, Wooldridge, editors. Volume 3.
5. Nonlinear Automatic Control by Gibson. McGraw Hill Book Co.
6. Electronic Engineering, "A Simple Automatic Extremum Seeker", March 1965, Volume 37 Number 445, pages 178, 179.

4.0 OPTIMUM CONTROLLER TECHNIQUES

The generalized design which is described in this section was arrived at after a close study of the Surveyor Battery Charge Regulator and also research into different types of optimum control circuits.

There are two basic procedures to obtain optimum performance (a minimum or maximum). The open loop approach makes use of knowledge the designer has about the system, however unexpected variations result in a deviation from the optimum. The closed loop approach makes use of measured data in order to learn what the optimum is and is relatively unaffected by changes (provided no saturation effects occur). The ability of the closed loop approach to continuously learn gives it a distinct advantage over the open loop approach in a changing system environment.

This section will compare the open loop and closed loop type controls in a qualitative manner. A simple block diagram for the open loop approach is shown in figure 4-1 and the block diagram for the closed loop approach is shown in figure 4-2. In the open loop approach, the model obtains information about the solar array and the battery to

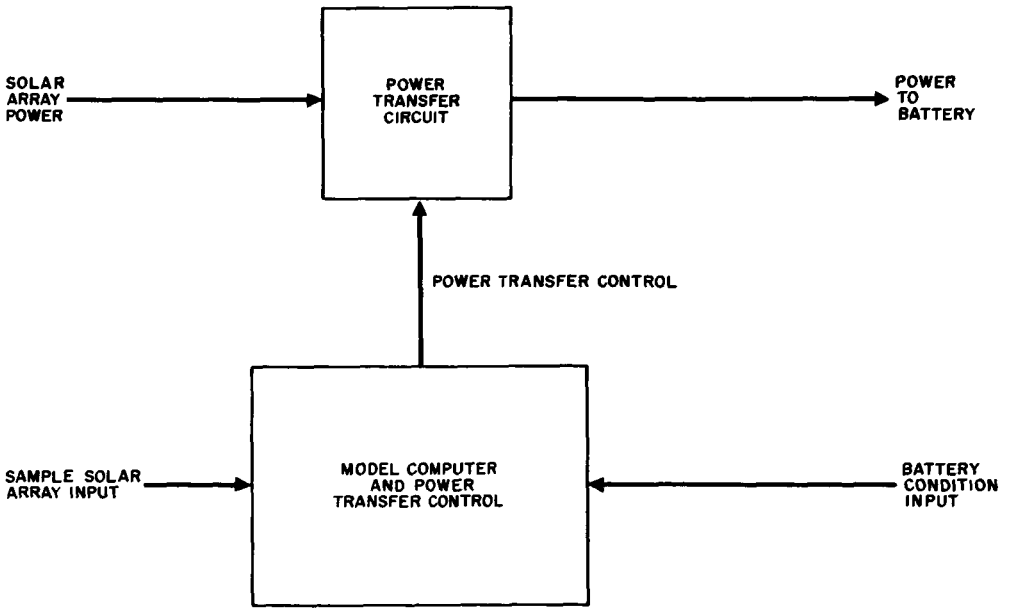

Figure 4-1. Open loop type control block diagram.

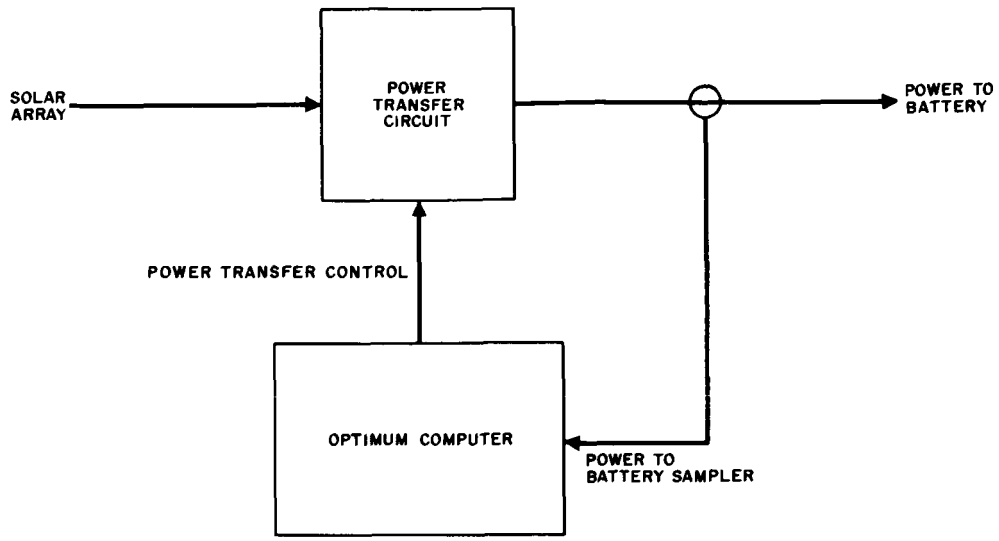

Figure 4-2. Closed loop control block diagram.

control the power transfer circuit. In the closed loop approach, a sample of the output power is obtained (the desired quantity) and the output power is maximized by the optimum controller determining the power transfer circuit.

4.1 OPEN LOOP TYPE CONTROL

4.1.1 Type 1: Model Comparator

The type 1 controller would use a model of the system and determine the systems performance by monitoring the system parameters. Since the true system has parameters varying such as solar panel temperature, intensity, age, and the state of charge plus the battery load, the system model would have to be quite complex. A very close approximation to a true model of the solar array is obtained by placing test solar cells in the array. However the problem of tracking, aging and of simulating shadowing effects is difficult to duplicate 100%. This type of control should yield results about the same as the closed loop systems that will be discussed later and is probably as complex.

4.1.2 Type 2: Battery Compensated Controller

A second type of open loop control would be to set the circuit to couple the optimum power for a typical solar panel condition. The battery voltage could easily be programmed back to correct for battery changes. If the solar array was always to be operated at one condition and aging is negligible, then this will yield a simple and satisfactory solution. This is actually a simple comparison model.

4.1.3 Type 3: Series and/or Shunt Coupling

The series and shunt type controls are included as a part of this report because of their present usage and not because they are optimum. The series type control is used to connect the solar array to the battery when charging is required and is the control element to limit charge. The shunt type control drains away the excess current from the battery whenever the full charge condition is reached. Neither technique serves to couple the maximum available power from the solar array to the battery and both have large dissipations at charge termination.

4.2 CLOSED LOOP TYPE CONTROL

4.2.1 Test Oscillator

The controllers using a test oscillator all operate on the principle that there is a sign change in gain as the maximum point is crossed. The feedback loop causes the varied parameter to change its value till the system comes into equilibrium about the maximum point. The chief disadvantage of this type of controller is that the response to changes would be relatively slow. For the spin stabilized type solar arrays this could be an extremely difficult problem to cope with.

4.2.2 Self Oscillating

This type of controller makes use of the entire feedback loop as an oscillator. Bi-stable action causes the varied parameter to be either increased or decreased. Each time the maximum point has

been passed by a pre-set amount the direction of parameter variation is changed. At least two methods for detection of the maximum crossing point exist. The first is a differentiating circuit which has the disadvantage of noise susceptibility. The second approach is to charge a capacitor to the peak value and compare this value to the existing value. This type of circuit has greater noise immunity. Since the switching power transfer circuit acts as a large signal noise generator, noise immunity is an important consideration. The self oscillating feedback loop with the peak holding detector are explained in detail later in this report.

4.3 BATTERY CONSIDERATIONS FOR CIRCUIT DESIGN

The section will be concerned with the general characteristics of a spacecraft type battery and the charge termination and limiting techniques to be used.

4.3.1 Battery Characteristics

There are two main assumptions that will be made concerning the performance of the battery. First, the battery voltage for any short period (0.1 second) is constant and second the battery voltage has a finite range of values. By assuming the battery voltage to be constant, the switching power transfer circuit's output current can be measured to reflect the output power. This will reduce the problem of measuring the output performance. It is necessary to know the output voltage range in order to properly design the switching power transfer circuit.

4.3.2 Battery Charge Termination and Limiting

There are two main methods for terminating the charge on a battery. They are linear control and turn off control.

4.3.2.1 Linear Control. The linear type control causes the battery charge to be decreased in accordance with a measured parameter. This

type control may be used to trickle charge the battery or to limit the charge to a safe current level. Effectively the trickle charge results in a constant battery voltage.

4.3.2.2 Turn Off Control. This type of control will result in the battery charge being stopped upon reaching the threshold of a given parameter. Typically this type of control is used for pressure sensing, since continuing the charge may be destructive.

4.4 SOLAR ARRAY CONSIDERATIONS FOR CIRCUIT DESIGN

4.4.1 Typical Solar Array Characteristics

A set of curves for a typical solar array is shown in Figure 4-3 and Figure 4-4. Both sets of curves are unitized with respect to the voltages and currents at the maximum power point. The maximum power point was chosen as the reference since the open circuit voltage and short circuit current have very little meaning to the dynamic circuit design considerations.

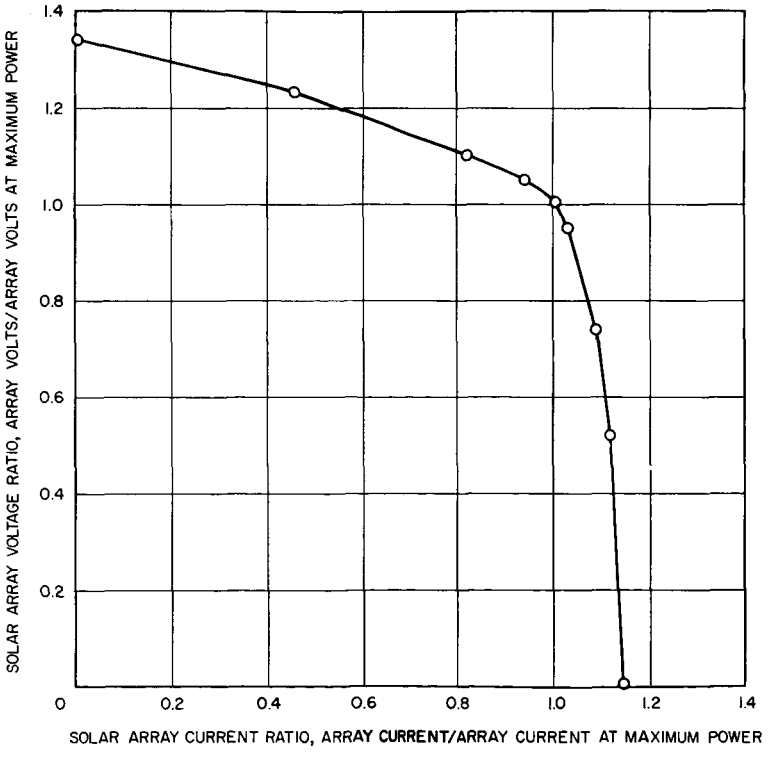

Figure 4-3. Solar array characteristics.

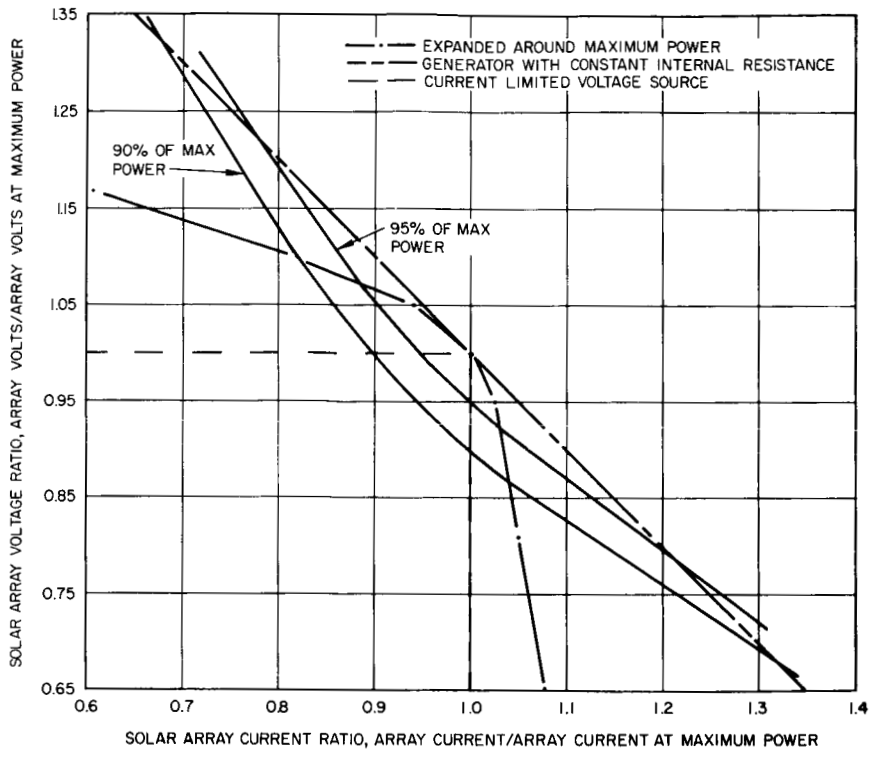

Figure 4-4. Solar array characteristics.

Figure 4-3 is a typical curve for a solar array and deviations from this curve should be anticipated. The deviations may result from state of the art improvement in the solar cell or they may result from aging effects or curves being taken at different temperatures. For purposes of analysis, these deviations will be considered zero and Figure 4-4 will be used as a universal solar array curve. The curve is taken from the power sources portion of this study.

Figure 4-4 is an expanded scale graph of Figure 4-3 in the vicinity of the maximum power point. In addition to the solar array curves, there are curves for a voltage source with a constant internal resistance and a current limited voltage source. All three curves shown have the same maximum power. In addition to the maximum power, locuses of the 90 percent and 95 percent of maximum power are shown. In analyzing the effect of the solar array characteristics on the optimum controller's operation; all three curves will be utilized.

4.4.2 Solar Array Simulators

In obtaining a solar array simulator for breadboard evaluation a wide range of curves should be available in order to insure that the optimum controller is not susceptible to changes in the shape of the solar array curve as well as to changes in power level. For this reason, the simulator should have all the curves shown in Figure 4-4 for each power level. The output of the simulator to be accurate must have very little stored energy. This restriction generally eliminates the possibility of using commercially available power supplies. An adaptor for available power supplies or designing a simulator will probably be required.

An additional requirement of the solar array simulator is dynamic programming ability. This feature will allow the susceptibility of the circuit to be tested. Programming is also necessary to simulate spin stabilized solar arrays. This programming can be done by varying the short circuit current parameter.

4.5 ANALYSIS OF THE OPTIMUM CHARGE REGULATOR USING A SELF-OSCILLATING OPTIMUM CONTROLLER

4.5.1 Optimum Charge Regulator Function

The function of the Optimum Charge Regulator (OCR) is to monitor the output performance and to couple the maximum power into the battery. Since the voltage of a battery is relatively constant for short periods of time (0.1 seconds), the output current will be a measure of the output power.

The block diagram of the OCR is shown in Figure 4-5. In the optimum mode of operation, the optimum controller senses the output current (Io) and sends a signal (M) to the duty factor controller (DFC). The duty factor controller, in turn, controls the Switching Power Transfer Circuit (SPTC) by controlling the duty factor (D). It will be shown in the circuit design portion of this report, that by controlling the duty factor of the SPTC the output current can be controlled. The OCR is, therefore, a closed loop control system.

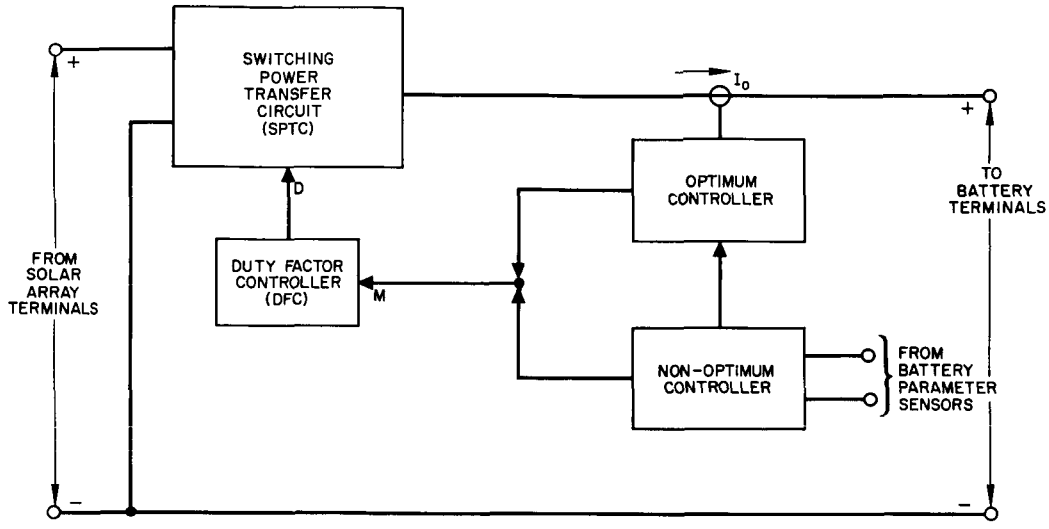

Figure 4-5. Block diagram of an Optimum Charge Regulator (OCR).

A non-optimum type controller is used to limit the charge or to limit the rate of charging of the battery. The non-optimum controller will sense the appropriate battery parameter and disable the optimum controller when the critical level has been reached. For linear type controls, it will then take over control of the M signal to the duty factor controller and control the output current. Linear control refers to the fact that the measured battery parameter will control the magnitude of output current.

4.5.2 Self-Oscillating Optimum Controller (SOC) Function

The function of the optimum controller is to monitor I_o and produce a signal M which will result in I_o being at its maximum value. Figure 4-5 is a block diagram for the optimum charge regulator and Figure 4-6 is a block diagram for the Self-Oscillating Optimum Controller. Figure 4-6 is an expansion of an optimum controller that is described in Figure 4-5.

In the self-oscillating optimum controller, the output current (I_o) is sensed and amplified to yield a voltage signal (A). The (A) signal goes to the peak holding and comparator block which charges a capacitor to the peak value ($\bar{A}$). As $\bar{A}$-A reaches the monitored comparator

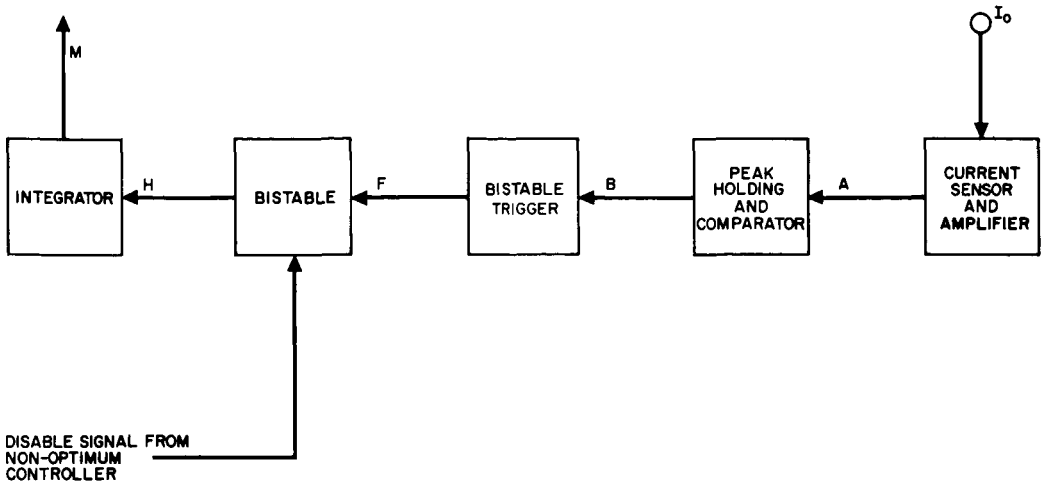

Figure 4-6. Block diagram of a Self-oscillating Optimum Controller (SOC).

pre-set value, a signal (B) is sent to the bistable trigger circuit. The bistable trigger produces a signal (F) to change the state of the bistable. The bistable generates a positive or negative signal (H) with respect to the integrator and the integrator produces a ramp signal $\left(\frac{dM}{dt}\right)$ having a positive or negative slope. During one half of a cycle, the slope will be positive and the other half cycle the slope is negative. In this way, each time $\bar{A}$-A reaches its pre-set value the sign of dM/dt is reversed.

The oscillation is produced by having M increase until the maximum point has been passed by the pre-set amount. Then M decreases until the maximum point has been passed by the pre-set amount again which causes M to again increase. In this manner, I_o is always close to its maximum value.

4.5.3 OCR/SOC Operation

In Figure 4-5 and Figure 4-6 the block diagrams for the OCR and SOC are shown. The letter designation for signals that are identified on these diagrams will be used throughout this report.

The basic scheme of operation will first be explained by an analog using a human operator. By employing a variable voltage source

for the M signal and an ammeter for the output current (Io) indicator, a human operator may control the output power. The maximum power would be found by varying the M signal voltage source in the direction of increasing Io until the peak is reached and a decrease in current noted. The direction of varying the M signal voltage would then be reversed until the peak was crossed going in the opposite direction. By continuing this process, the maximum output power could be maintained even in a changing environment. The function of the human operator is identical to that of the optimum controller.

The waveforms for an idealized steady state cycle of the OCR are shown in Figure 4-7. A positive or negative H signal results in M decreasing or increasing, and a corresponding decrease or increase in D (duty factor). The D (duty factor) varying results in the average output current (Io) shown in Figure 4-7. The output current is composed of a DC or average value and an AC ripple current. The AC current is a result of the switching of the SPTC, and must be eliminated from the A signal in order to sense the maximum power effectively. When A decreases so that $\overline{A}$-A is at its pre-set difference level, a signal B is sent to the trigger which results in the F signal changing the H signals polarity. This scheme results in the output current oscillating about its maximum value.

In the upper left hand corner of Figure 4-7 a plot of I_o vs D is shown. The function is assumed to be parabolic in nature for the purpose of the analysis. A second shape will be assumed later in the report in order to demonstrate that the particular shape of the maximum is not critical and the differences are minor.

4.6 ANALYSIS OF THE OCR OPERATION

Before analyzing the operation of the OCR, a few terms will be defined. The hunting zone as shown in Figure 4-7 is the region of operation near the optimum point. The hunting is the process of seeking the maximum point. The hunting frequency is the number of complete hunting cycles per second. The hunting loss is the associated loss due to oscillating around the maximum point, and the hunting

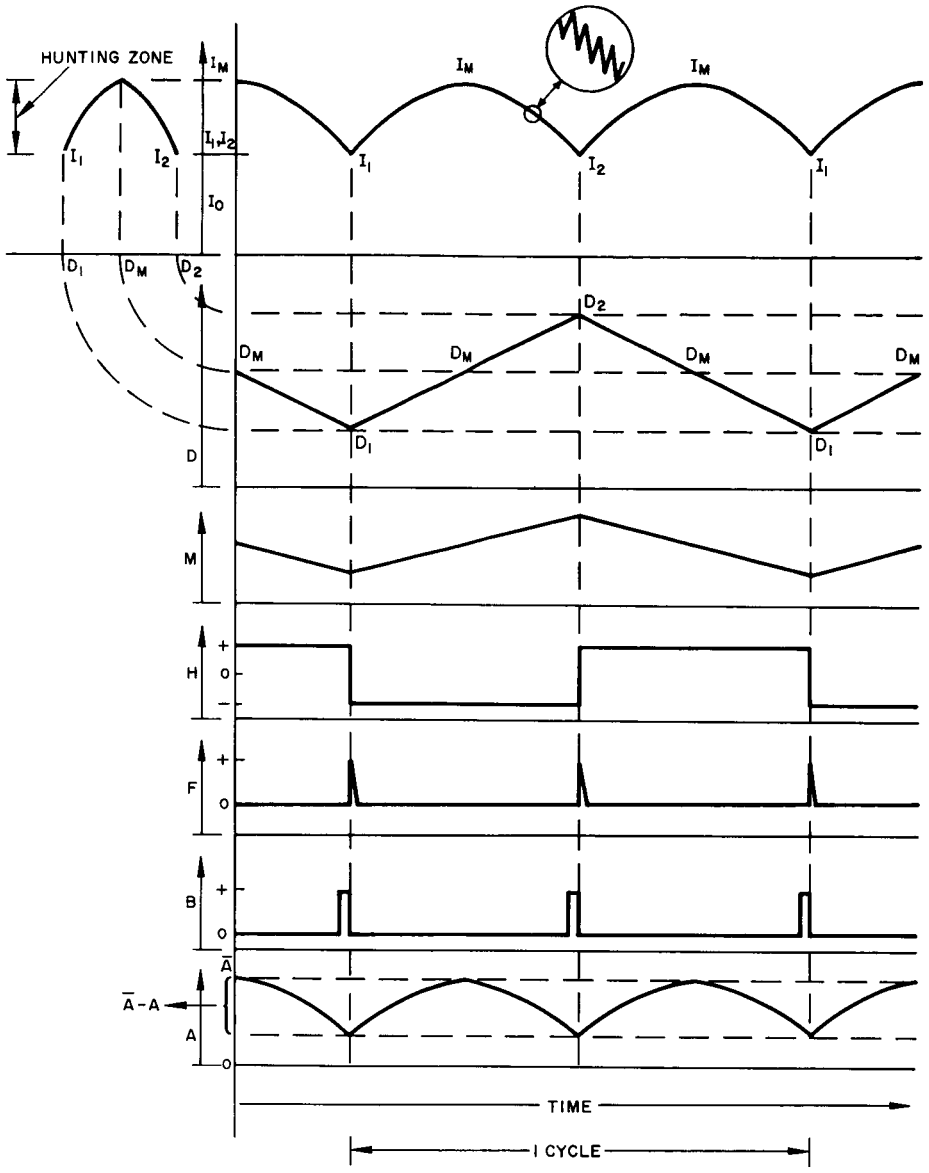

Figure 4-7. Idealized waveforms for OCR.

efficiency is the ratio of the average output to the maximum output expressed in percent for the solar array.

4.6.1 General Hunting Equation

Near the maximum power point, the following equation will be used to describe the output current variation as a function of duty factor.

$$I_o - I_M = - K_1 (D - D_M)^2$$

I_o is the output current

I_M is the maximum output current

K_1 is a constant dependent on solar array and battery parameters

D is the duty factor

D_M is the duty factor at the maximum output current.

4.6.2 Hunting Losses

From Figure 4-7 it will be assumed that $I_1 = I_2$ and $I_M - I_1 \equiv \Delta I$

$$I_{Ave} = I_M - \frac{1}{3} \Delta I$$

where

I_{Ave} is the average output current

$$P_{Ave} = E_B I_{Ave}$$

where P_{Ave} is the average output power and E_B is the battery voltage

$$P_{HL} = \frac{1}{3} E_B \Delta I$$

where P_{HL} is the hunting loss.

4.6.3 Hunting Frequency

Solving for D_1 and D_2 yields

$$D_1 = D_M - \sqrt{\Delta I / K_1}$$

$$D_2 = D_M + \sqrt{\Delta I / K_1}$$

assuming the following

$$\frac{dD}{dt} = K_2 \frac{dM}{dt} = K_3 H$$

where

K_3 is the appropriate integrator time constant and conversion constant

K_2 is the conversion constant

$$\int_{D_1}^{D_2} \frac{dD}{dt}\, dt = \int_{t_1}^{t_2} K_3 H\, dt$$

$$\Delta D \equiv D_2 - D_1 = K_3 H (t_2 - t_1)$$

$$t_2 - t_1 = \frac{2\sqrt{\Delta I / K_1}}{K_3 H}$$

$$f = \frac{1}{2(t_2 - t_1)} = \frac{K_3 H}{4\sqrt{I/K_1}} = \frac{K_3 H}{2(D_2 - D_1)} = \frac{K_3 H}{2\,\Delta D}$$

4.6.4 Using a Triangular Approximation

A second approximation will be used to calculate the hunting losses and frequency. This is done in order to get a feel for the accuracy of the approximation and to establish some worst case values for the OCR design. Figure 4-8 shows a similar set of idealized waveforms using the triangular approximation.

Assuming as before

$$I_1 = I_2$$

$$I_M - I_1 \equiv \Delta I$$

$$I_{AVE} = I_M - \frac{1}{2}\Delta I$$

= Average output current for a hunting cycle power output

$$P_{AVE} = E_B I_{AVE}$$

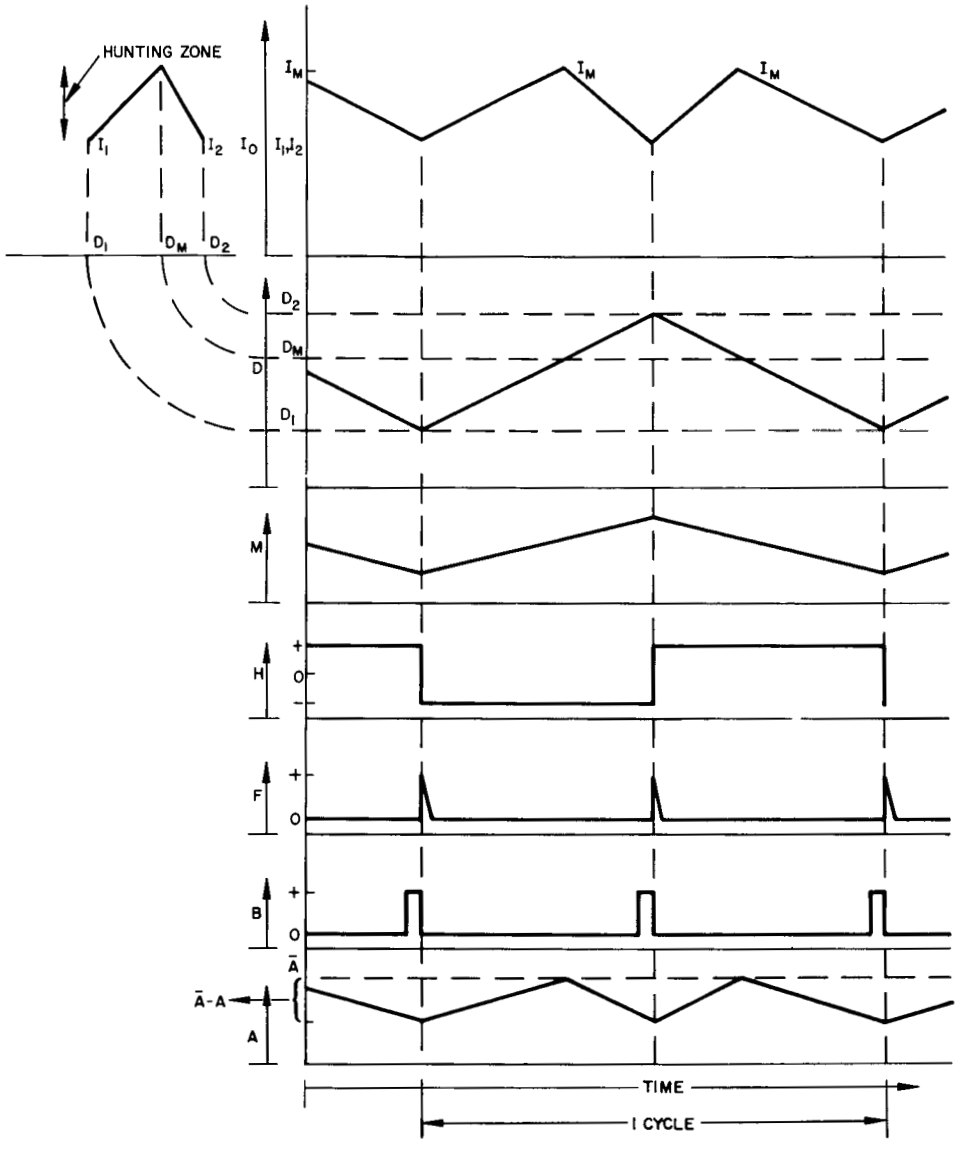

Figure 4-8. Triangular approximations for OCR waveforms.

$$P_{HL} = \frac{1}{2} E_B \Delta I = \text{hunting losses}$$

as before

$$\frac{dD}{dt} = K_2 \frac{dM}{dt} = K_3 H$$

therefore the frequency expression is the same

$$f = \frac{1}{2(t_2 - t_1)} = \frac{K_3 H}{2(D_2 - D_1)}$$

4.6.5 Summary of the General Hunting Equations

Before proceeding to analyze the effects of circuit losses and other dynamic effects, the equations will be summarized. For the symbols used refer to Section of 4.6.1 through 4.6.4. Only the worst case equation for the two approximations are shown.

$I_{AVE} = I_M - \frac{1}{2}\Delta I$ = average current during a hunting cycle

$P_{AVE} = E_B I_{AVE}$ = average power to the battery

$P_{HL} = \frac{1}{2} E_B \Delta I$ = average power lost in hunting

$f = \frac{K_3 H}{2 \Delta D}$ = hunting frequency

4.6.6 Time Delay Stability

The OCR will be considered stable if under steady state conditions the oscillation produced by the feedback loop is controlled by a reversing signal produced after the maximum point has been crossed. Similarly a reversal signal that is produced without passing the maximum point will be termed a false trigger and the operation must be considered unstable.

Figure 4-9 shows a simplified set of waveforms for the OCR with time delays. The time delay has been simplified to be between the output current sense (I_o) and the output of the current sensor and amplifier (A). A second time delay is considered to be between the peak holding and comparator output (B) and the bistable trigger output (F).

It will be assumed that the positive and negative slopes of A are equal in magnitude. This makes T_1 equal to T_4 and T_2 equal to T_3.

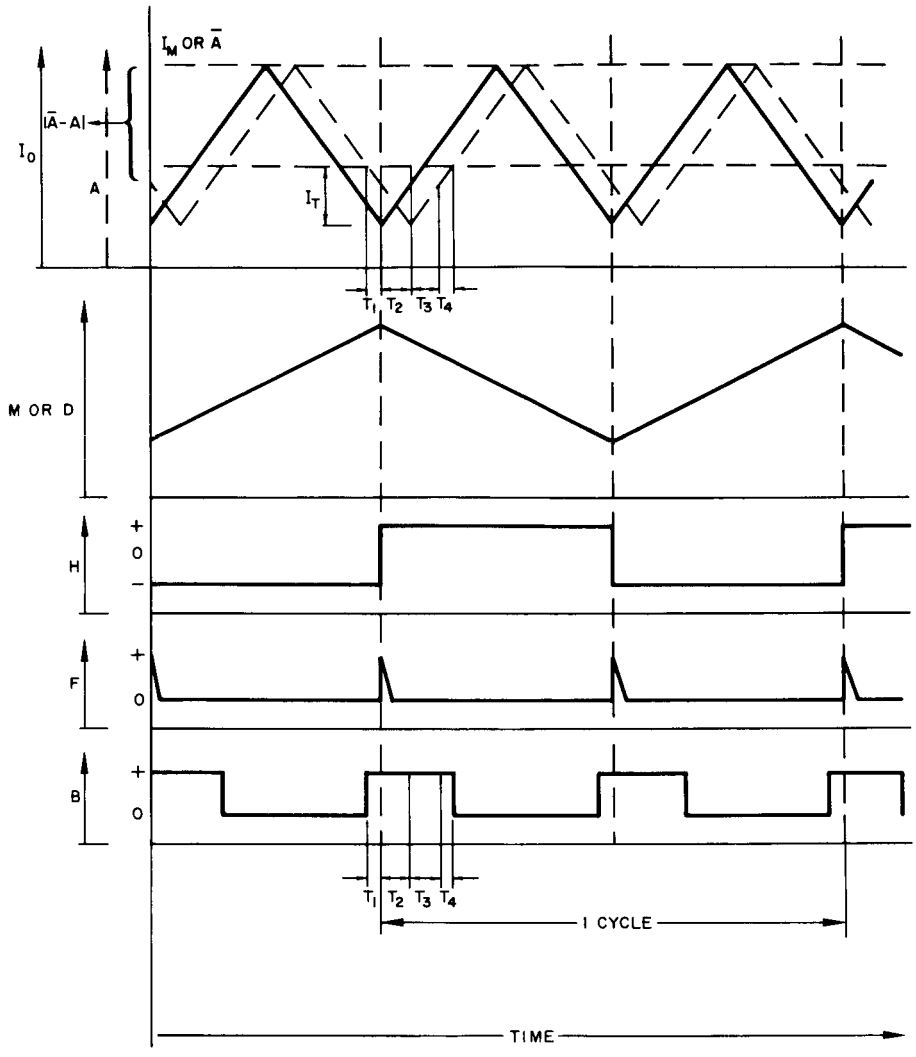

Figure 4-9. Waveforms for OCR with time delay.

The time delay between the B and F signals will be noted as T_{BF}, and T_2 is the time delay between the A and I_o signals. From Figure 4-9 the following equations can be arrived at for stability. The other assumption made is that the trigger can only put out one pulse each time it is triggered and that during T_{BF} no pulse may be put out. Therefore

$$T_{BF} = 2(T_1 + T_2)$$

The circuit is stable for T_1 greater than zero, an additional effect of the time delay is to increase the hunting losses. This may be calculated by adding the I_T shown in Figure 7 to the pre-set value of ΔI and substituting the sum into all equations. There are three basic methods of insuring stability due to time delay.

Method 1. Insert a lead network into the current sensor block. This approach will insure stability and will minimize ΔI which in turn minimizes the hunting losses.

Method 2. Each time an F signal is produced, use it to decrease $\bar{A}$. This must result in $\bar{A}$-A being below the pre-set value so that the B signal will vanish. This method has no effect on ΔI.

Method 3. Each time an F signal is generated, inhibit the B signal for a fixed time. This method has no effect on ΔI.

4.6.7 Memory Stability

In the previous section (under steady state conditions, the loop stability was defined as the oscillation produced by the feedback loop is controlled by a reversing signal produced after the maximum point has been crossed. Similarly if no reversal signal is produced after passing the maximum point it will be termed a loss of memory and such an operation must be considered unstable.

In order to be stable the following equation must hold:

$$\frac{d\bar{A}}{dt} \ll \frac{dA}{dt}$$

This condition is necessary so that $\bar{A}$-A may reach its pre-set value. An additional effect of $\bar{A}$ decreasing during the hunting cycle is to increase the hunting losses. Since A is proportional to I_o, the increase in the ΔI can be determined by computing the amount that $\bar{A}$ decreases.

4.6.8 Stall

When the circuit is initially started, $\bar{A}$ represents a zero current condition and $\bar{A}$-A will be unable to reach its pre-set value. This condition could exist forever if the bistable came on in the wrong position. This condition can be eliminated by making the bistable trigger circuit free run at a frequency much lower than the lowest hunting frequency. This will ensure starting of the hunting cycle.

4.6.9 Susceptibility to Battery Bus Voltage Changes

The susceptibility of the OCR will be defined as a condition that results in a reduced hunting efficiency and is produced by an external source.

In order to establish a criteria to determine the amount of AC voltage that can exist on the battery bus terminals without causing a reduced hunting efficiency, it is only necessary to recall that the OCR senses a pre-set ΔI of current change in controlling the hunting cycle. If the AC voltage results in a change in sensed current equal in magnitude to the pre-set value, it is obvious that the external source will have about the same influence on the control loop as the internal controlling scheme. It will be assumed for design purposes that an equal influence is undesirable. For design purposes, it will be assumed that the sensed current change of the external source should be less than half the pre-set ΔI. This allows the normal hunting cycle to be relatively unaffected by external sources.

By assuming a constant circuit efficiency the following equation can be derived:

$$\Delta e_B = \frac{E_B}{I_o} \Delta I$$

I_o is the OCR output current

E_B is the battery voltage

The maximum Δe_B that will be permitted for design purposes is given by the following equation:

$$\Delta e_{B\ max} = \frac{E_B}{I_B} \cdot \frac{\Delta I}{2}$$

The above equation for Δe_B maximum does not account for any influence of frequency on the level of susceptibility. For the changes that take place over a period of time covering many hunting cycles the criteria obviously cannot hold. In addition, the changes in battery bus voltage that take place at very high frequencies will be eliminated by the required filtering in the sensing amplifier. Therefore, it may be concluded that the expression for Δe_B max holds in the frequency range of the hunting frequency and it will increase outside this frequency range.

4.6.10 Susceptibility to Solar Array Changes

The susceptibility for the OCR was defined in the preceding section. Using the same criteria yields the following equation:

$$\Delta P_{SA\ MAX} = \frac{E_B \cdot \Delta I/2}{2}$$

ΔP_{SA} is the change of solar array power

The applicable frequency is again in the range of the hunting frequency. For frequencies above or below the hunting frequency range the ΔP_{SA} max increases.

4.6.11 Noise Effects

One of the limiting criteria for the sensitivity of any type of electronic circuit is the noise level. In this case the effects of random noise will be neglected due to the high value of noise produced by the switching power transfer circuit. The primary component of the AC signal occurs at the switching frequency and must be taken into account in the circuit design in order to determine the signal to noise ratio of the sensing circuit.

4.7 MODIFICATIONS TO THE BASIC SCHEME

4.7.1 Transient Response Improvement

One of the conditions for stable operation is to design $\bar{A}$ with a long time constant. $\bar{A}$ having a long time constant will result in a long settling time for changes in battery or solar array conditions. This situation can be improved by use of a non-linear amplifier. The non-linear amplifier would serve to rapidly charge or discharge the peak holding capacitor. Thus $\bar{A}$ would be made to approach its value rapidly and to change its value rapidly only when the pre-set value of ΔI has been exceeded. By this modification it is possible to have a long $\bar{A}$ time constant and to have a good transient response.

4.7.2 Reducing Hunting Losses

It was shown that the hunting losses are proportional to pre-set ΔI. However, it was also shown that the susceptibility of the unit to external signals was proportional to the pre-set ΔI. That is the larger the ΔI the less influence the external signals will have on the hunting operation. This must result in a compromise between the hunting losses and the susceptibility.

A possible solution to reduce the effects of the compromise would be to allow the H signal to take on two magnitudes. A low magnitude when the hunting cycle is near the maximum point and a high magnitude when the hunting cycle is near the pre-set ΔI or far from the maximum point. Since the change of D with respect to time is proportional to the H signal, the output current will be near the maximum for a greater percentage of time. This will result in the hunting loss being reduced and the susceptibility being approximately the same for a given ΔI.

4.8 REVIEW OF DESIGN PARAMETERS AND TRADEOFFS

This section will review the parameters that affect the design of the self-oscillating optimum controller, and will point out the tradeoffs that can be made.

4.8.1 Frequencies

There are three frequencies associated with the operation of the optimum charge regulator. One is the free running frequency of the bistable trigger circuit (f_B). The only requirement of this frequency is that it must be sufficiently lower than the hunting frequency so as not to interfere with the control loop. The only reason for using a free running circuit is to provide a positive mechanism for starting.

The second frequency to be considered is the hunting frequency (f_h). This frequency is dependent on the battery and solar array voltages for its value. As a result, the hunting frequency will have a relatively wide range of values.

The third frequency is that of the switching power transfer circuit (f_s). This frequency has AC components which act as interference to the normal hunting process, and therefore must be filtered out of the sensed signal. The f_s frequency must be higher than f_h because of this filter requirement. The difference between the two frequencies will be a function of the pre-set ΔI and filter (phase shift) characteristics.

4.8.2 Stability

There are two distinct requirements for a stable hunting frequency.

The first requirement considers the phase shifts or time delays in the control loop. This phase shift will result in additional hunting losses as well as instability. The phase shift can be minimized by making the ratio of f_s/f_h as high as possible.

The second requirement considers the peak holding or memory capacitor. This requirement essentially states that the capacitor should not be discharged appreciably during each hunting cycle. The discharge of this capacitor must also be considered in determining the hunting losses. Therefore, a very long time constant should be used with the speed up scheme described in Section 4.7.2 used to provide good transient response.

4.8.3 Susceptibility

The susceptibility to either solar array power changes or to battery voltage changes is proportional to the pre-set ΔI in the range of the hunting frequency. Outside the hunting frequency range the level of signal is increased by the ability of the control loop to respond at frequencies below the hunting frequency and by the filter components at frequencies above the hunting frequency. A compromise between hunting losses and susceptibility must be made in order to have a proper working unit in a full system environment.

4.9 GENERALIZED CIRCUIT DESIGN

This section will be concerned with the general types of circuits that can be used to fill each of the blocks shown in Figure 4-10. The waveforms for these blocks are shown in Figures 4-7 through 4-9.

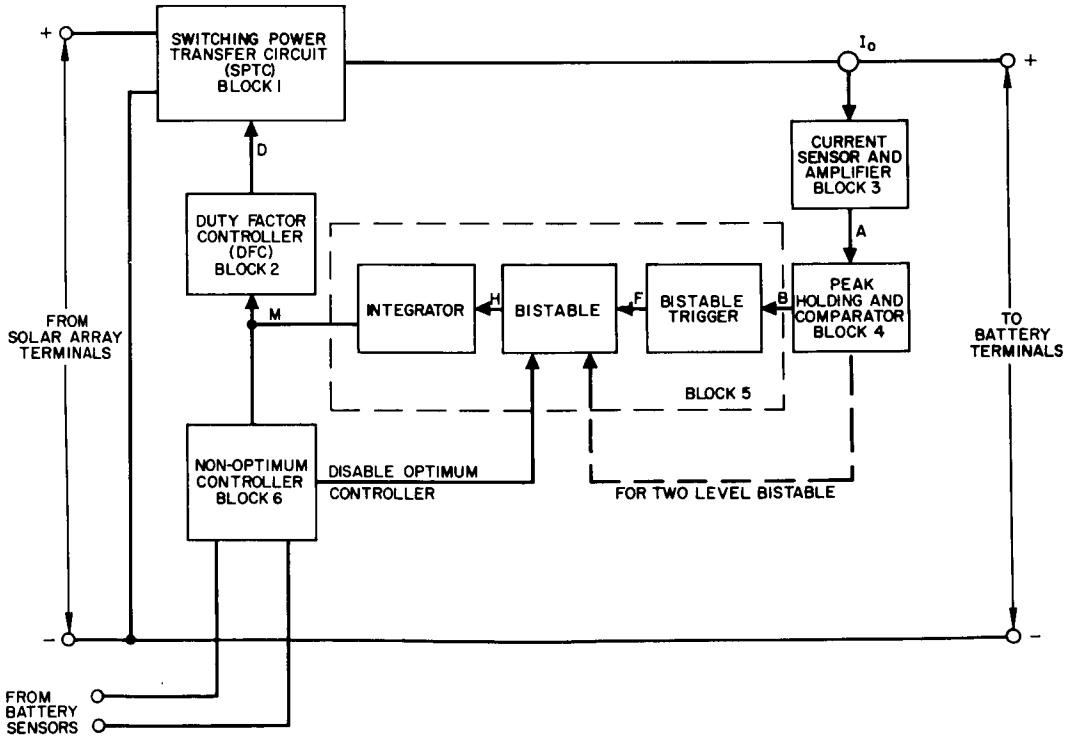

Figure 4-10. Block diagram for OCR using a SOC.

4.9.1 Switching Power Transfer Circuitry (Block 1)

Two distinctly different types of circuits will be discussed for transferring power from the solar array to the battery. The discussion on the step down SPTC will be limited to a qualitative assessment, and the switching choke type SPTC will be analyzed. The switching choke type will be used in both Case I and Case II studies. The SPTC is used to transfer power efficiently from the solar array to the battery.

4.9.1.1 Step-down SPTC. The essential components for the Step down SPTC are shown in Figure 4-11. The purpose of components L1, C1, and C2 are to filter the switching currents produced by transistor Q1. This filter allows the solar array to operate at one point on the solar array curve for a given duty factor. Because of this filter, close to 100 percent of the solar array power may be transferred to the battery. Transistor Q1 and diode CR1 act to switch the input of choke L2 to either the solar array voltage or to the return voltage. The choke L2 acts as an efficient energy transfer mechanism to the battery. Capacitor C3 represents the output filter and acts to keep the SPTC noise from getting to the battery plus it serves to decouple any noise on the battery from the OCR circuitry. This type of SPTC was used on the

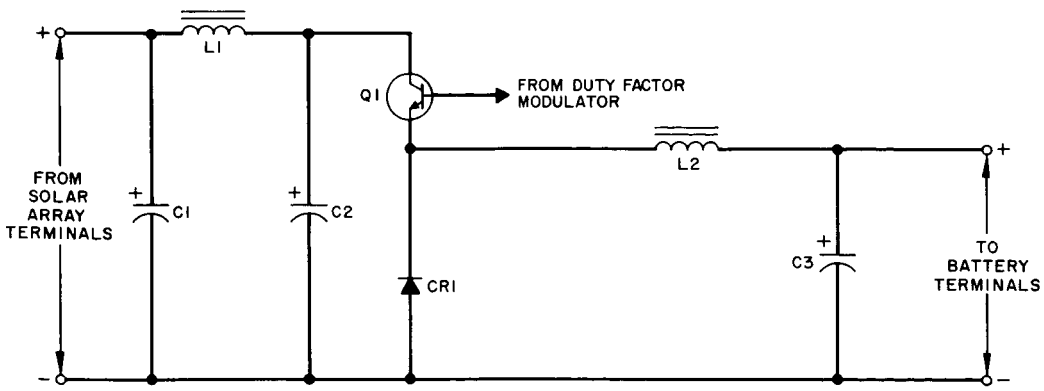

Figure 4-11. Step down SPTC.

Surveyor program since the solar array maximum power voltage was always sufficiently greater than the battery voltage to allow good operation.

4.9.1.2 Switching Choke (SPTC). The switching choke SPTC is shown in Figure 4-12. The input filter consisting of components L1, C1 and C2 performs the same function as in the step down SPTC. The main difference between the two SPTC circuits comes in the energy transfer mechanism. In this circuit the main choke has two windings. The energy is stored in the choke by turning on transistor Q1 using the primary winding (P). When transistor Q1 is turned off, the secondary winding(s) will release the energy stored in the choke through diode CR1 into the battery terminals. The output filter is represented by capacitor C4 and prevents the undesirable noise from passing into or out of the OCR. Capacitor C3 protects transistor Q1 from its switching transients.

4.9.1.3 Analysis of the Switching Choke SPTC. The first step is to define the duty factor. The D1 duty factor applies to the conduction of transistor Q1 and is defined as the ratio of on time to the time of a complete cycle. The D2 duty factor applies to the conduction of diode

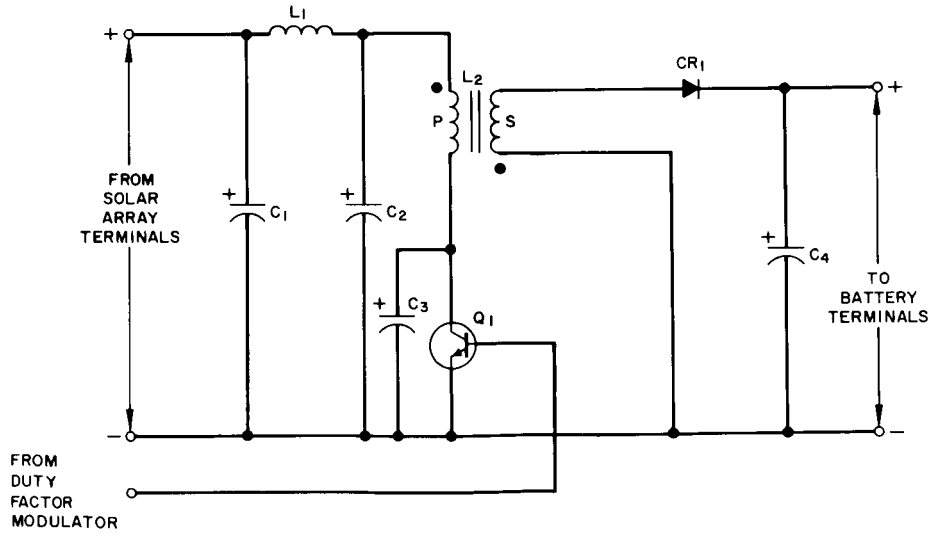

Figure 4-12. Switching choke SPTC.

CR1 and again is defined as the ratio of the on (conducting) time to the time of a complete cycle.

$$D_1 = \frac{T_1}{T_T}$$

$$D_2 = \frac{T_2}{T_T}$$

D_1 is the duty factor of Q1

D_2 is the duty factor of CR1

T_1, T_2 is the appropriate on time

T_T is the time for a complete cycle.

In order to allow the choke to be completely discharged each cycle, the following equation will hold:

$$D_1 + D_2 \leq 1$$

By restricting D1 and D2 to be each less than 0.5 under all conditions the best compromise between input and output ripple will be achieved. In addition the SPTC will have a minimum response time. By using the equation

$$E = L \frac{di'}{dt}$$

and the previously defined duty factor equations, the equations shown in the table in Figure 4-13 can be derived for the input and output circuits.

L_p is the inductance of the primary and Ls is the inductance of the secondary on the switching choke. The I_1 is the amount of current passing through Lp when the switch is turned off and I_2 is the current that will be passing through Ls immediately after the transistor is turned off. This assumes that the choke has been allowed to completely discharge when discharging into the battery. I_o is the average current going to the battery and I_s is the average current being drawn from the solar array.

SWITCHING CHOKE SPTC EQUATIONS

INPUT	OUTPUT
$f_S \equiv \frac{1}{T_T}$	$f_S \equiv \frac{1}{T_T}$
$D_1 \equiv \frac{T_1}{T_T} = T_1 f_S$	$D_2 \equiv \frac{T_2}{T_T} = T_2 f_S$
$\Delta I_1 = \frac{E_{SA} D_1}{L_P f_S}$	$\Delta I_2 = \frac{E_B D_2}{L_S f_S}$
$I_{SA} = \frac{E_{SA}}{2 L_P f_S} D_1^2$	$I_O = \frac{E_B}{2 L_S f_S} D_2^2$
$P_{SA} = \frac{E_{SA}^2 D_1^2}{2 L_P f_S}$	$P_B = \frac{E_B^2 D_2^2}{2 L_P f_S}$

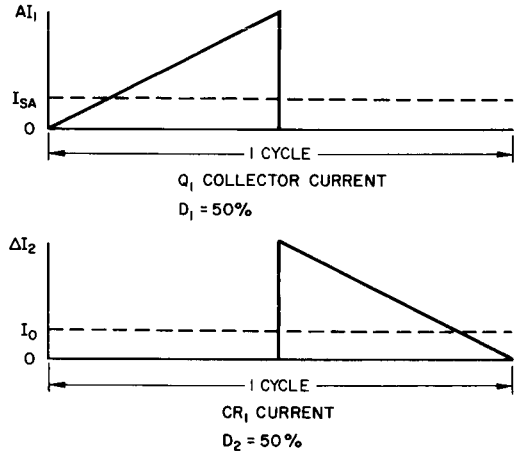

Figure 4-13. Switching choke SPTC — equations and current waveforms.

The effects of the input filter are assumed to be negligible. Since D1 is the duty factor controlled by the duty factor modulator, a point by point calculation can be made for the output current for each assumed solar array condition.

The current waveforms for the collector of transistor Q1 and the diode CR1 are also shown in Figure 4-13. As can be seen by these simple examples, the ripple current on both the input and output have the same relative magnitude. Both ripple currents are high and represent a filtering problem. However by paralleling circuits as shown in Figure 4-14 and turning on the transistors (Q1-A and Q1-B) on alternate half cycles, both the input and output ripple will be reduced. This reduction of ripple is graphically shown in Figure 4-15. Each parallel branch will be called a phase. By increasing the number of

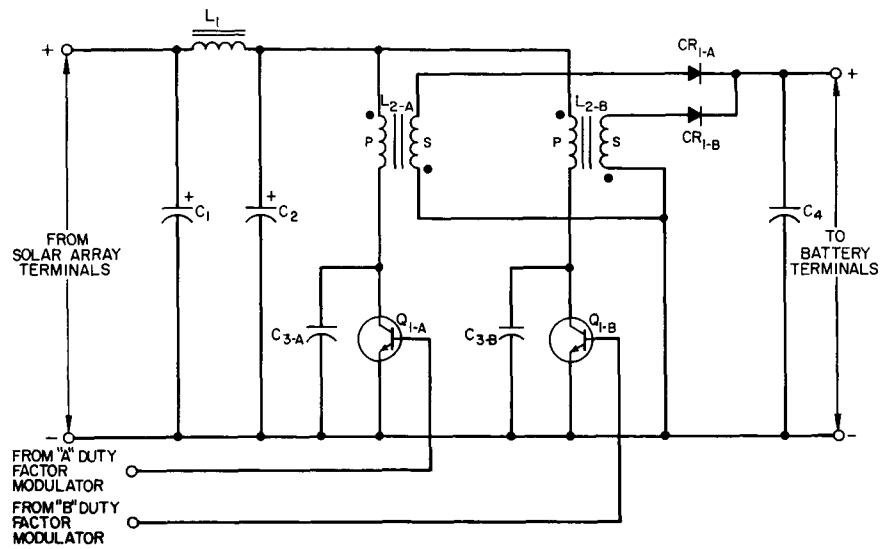

Figure 4-14. Two Phase Switching Choke SPTC

phases the input and output ripple could be reduced still further. In this way, ripple magnitude may be traded for switching circuit complexity.

4.9.2 Duty Factor Controller Circuitry (Block 2)

The duty factor for a multi-phase switching choke SPTC has two basic requirements. The first requirement is control of the on time for each switch and the second requirement is to turn on the switches at equally spaced time intervals. It is also best for the switching frequency to be independent of duty factor in order to optimize the design of the input and output filters. A basic circuit that is capable of performing these functions is shown in Figure 4-16. Each phase output is sent through an amplifier before going to the SPTC. This allows the Duty Factor Modulator and Controlling circuit to operate on a low power consumption. Figure 4-17 is a logic diagram for a 4 phase system which will be used in the Case II study.

4.9.3 Optimum Controller Circuitry

The optimum controller is made up of the functions shown in Figure 4-6. The circuits discussed in the following sections are typical of those that will be used for the case studies.

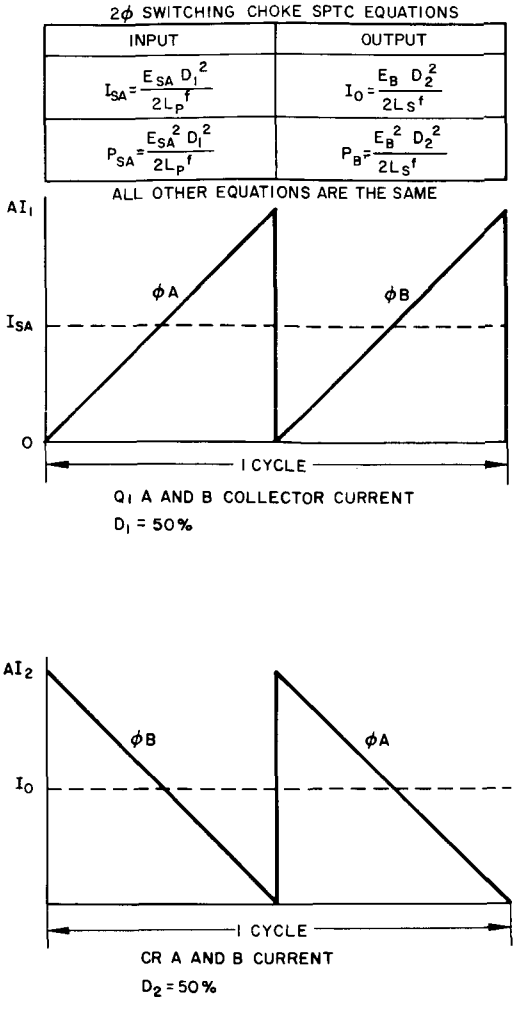

Figure 4-15. 2φ switching choke SPTC.

4.9.3.1 Current Sensor and Amplifier Circuit (Block 3). There are two basic approaches to sense current. A mag-amp approach has the ability to amplify and introduce almost no losses into the sensed circuit. The second approach is to sense a voltage drop across a known resistance. The total power consumed by both techniques is about the same, and the resistance measurement will be selected because of its flexibility. A typical sensing circuit is shown in Figure 4-18. As can be seen from the circuit, the power losses in the current shunt can be traded for amplifier circuit complexity.

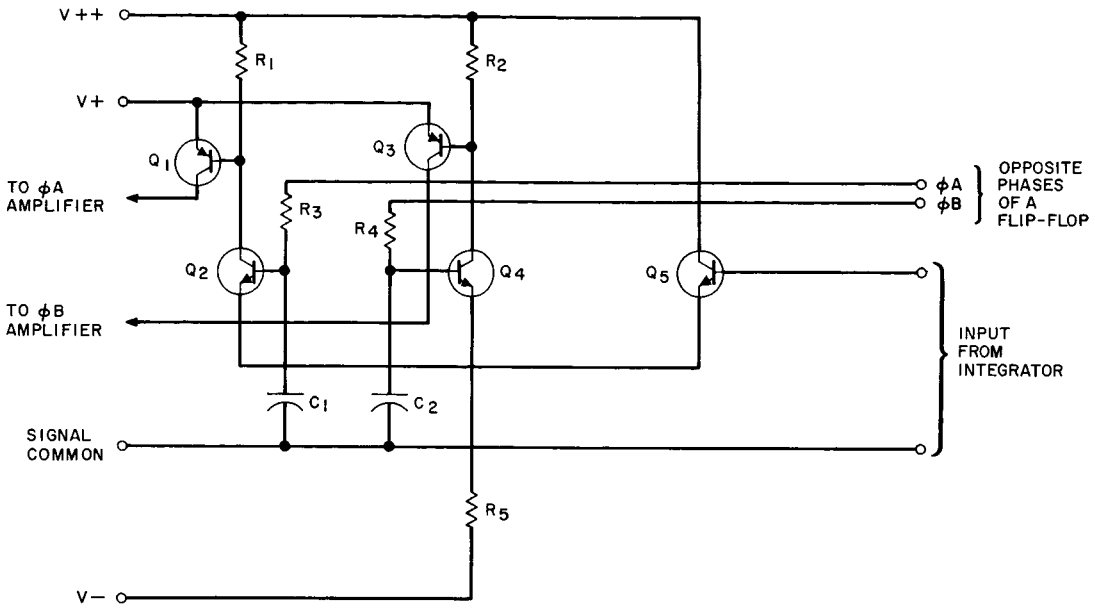

Figure 4-16. Duty factor modulator for 2φ SPTC.

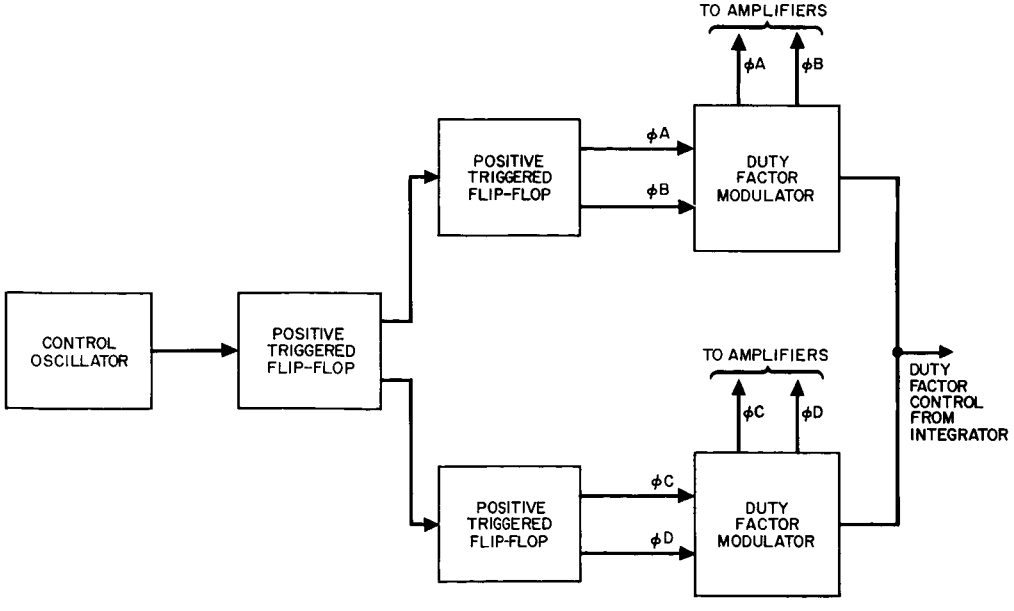

Figure 4-17. Logic diagram for a 4φ duty factor modulator.

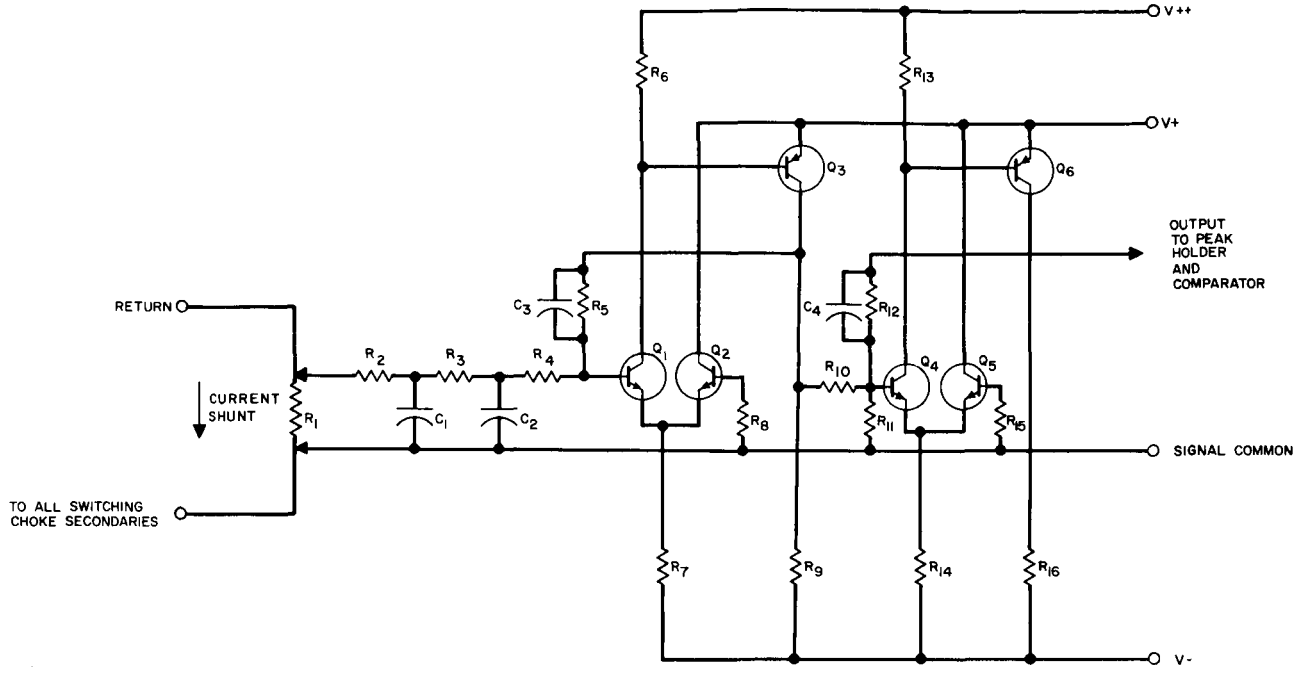

Figure 4-18. Current sensing and amplifier.

4.9.3.2 Peak Holding and Comparator Circuit (Block 4). A peak holding and comparator circuit is shown in Figure 4-19. Capacitor C1 in the circuit is charged to the positive peak value of the input signal. When the input decreases, transistors Q4 and Q2 are turned on and in turn will turn on transistors Q9, Q8, and Q7. Transistors Q9, Q8, and Q7 are set to come on at slightly different levels in order to perform their respective functions.

4.9.3.3 Trigger, Bistable, and Integrator (Block 5). The trigger, bistable, and integrator circuits are shown in Figure 4-20. Transistor Q2 is the trigger (blocking oscillator) amplifier. The output of the blocking oscillator is used to change the state of the bistable (Q3 and Q4) and to turn on transistor Q1 which inhibits the trigger signal for a fixed time. This allows the trigger time constant of the blocking oscillator to be short since the inhibit period will prevent a false

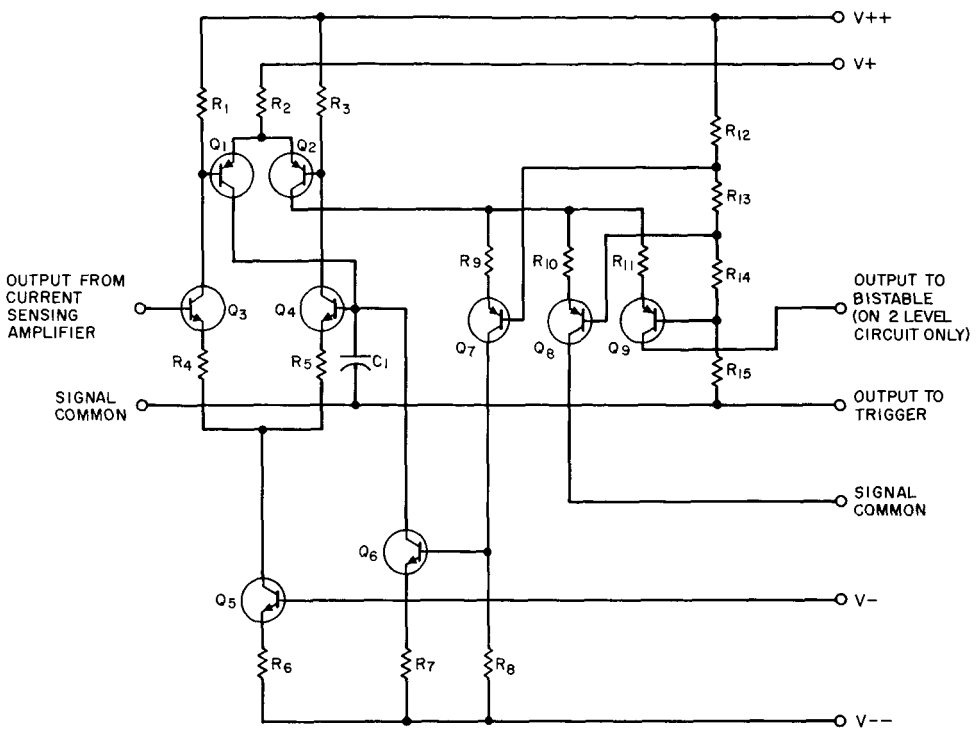

Figure 4-19. Peak holding and comparator.

trigger. The bistable consisting of transistors Q3 and Q4 drives the integrator differentially. The integrator time constant consists of R13 and C6. The differential operational amplifier consists of transistors Q5, Q6 and Q7. An alternate bistable is shown in Figure 4-21. In this bistable, the voltage being applied to the input of the integrator can be varied by a signal from the peak holding and comparator circuit.

4.9.4 Non-Optimum Controller

No circuits are shown for a typical non-optimum type of control. The circuits for this type of function can act in two basic modes. The first occurs if the parameter has been reached to turn off the circuit. This can be done by sending a signal to the bistable to force a zero percent duty cycle. The second type of circuit results in a linear control. This can also be done by sending a signal to the bistable to force

a zero percent duty cycle and with a second signal control the duty factor.

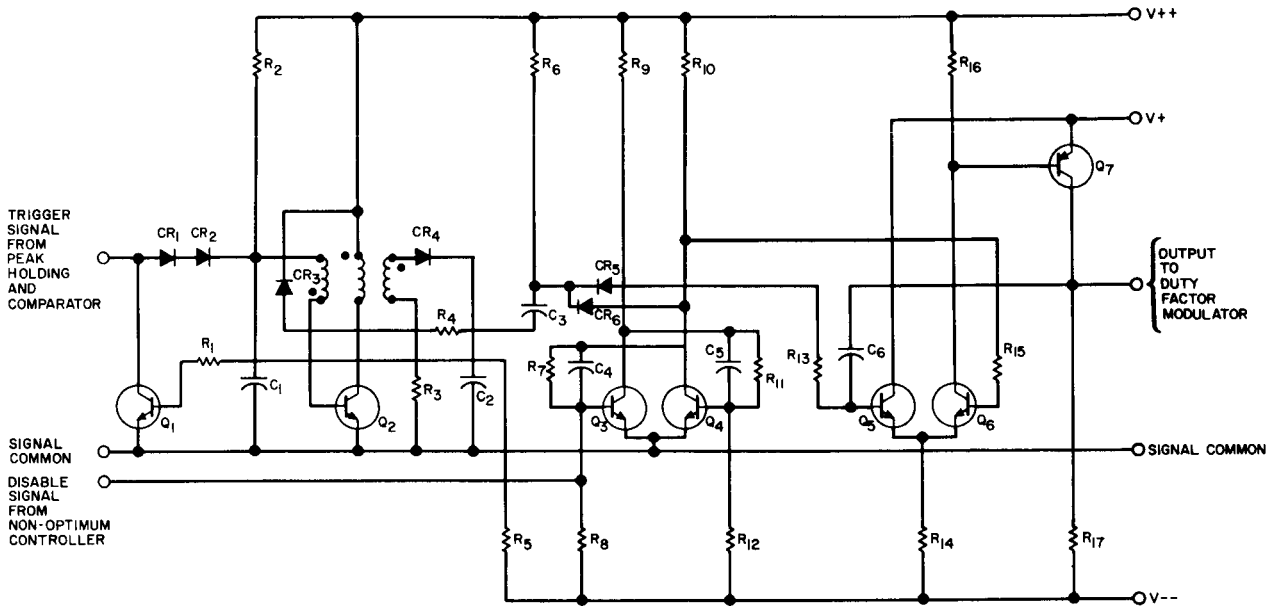

Figure 4-20. Trigger, bistable, and integrator (simple bistable only).

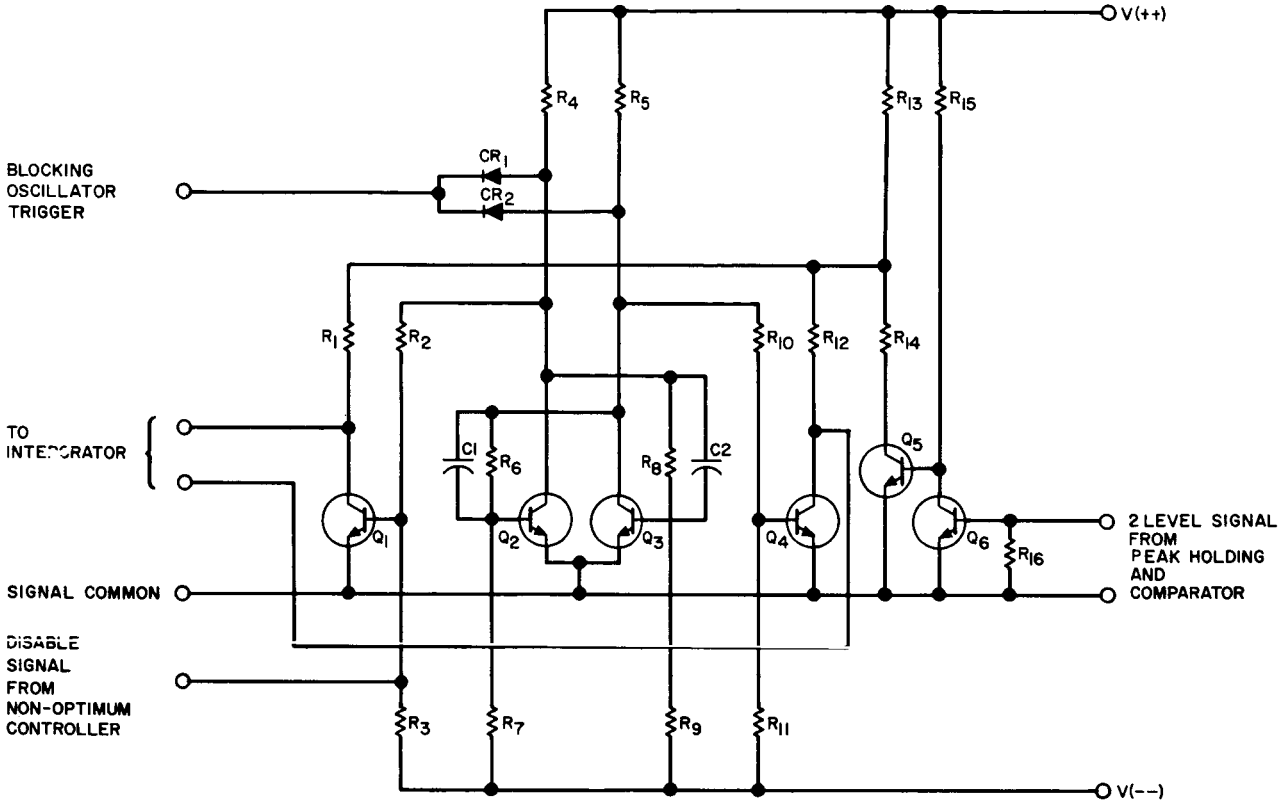

Figure 4-21. Modified bistable for 2 level control.

5.0 BATTERY AND SOLAR ARRAY CHARACTERISTICS

The major effort during the first quarter was spent in research and study of battery systems to be used for both spin stabilized and oriented prime power solar array systems.

Special consideration was given to sensing of battery state-of-charge and use of battery internal control devices to permit optimized charging.

5.1 CASE I

This involves the use of a spin stabilized satellite in a highly elliptical earth orbit. Approximately 50 watts of power are available at the solar panel output terminals. Output voltage will range from 12 to 20 volts.

The orbital periods for Case I are summarized below:

Orbit	A	B
Apogee	100,000 mi.	200,000 mi.
Perigee	200 mi.	1,000 mi.
Orbital Period	87.5 hrs	234 hrs
Dark time/orbit	0.5 hrs	16 hrs
Charge time/orbit	87 hrs	218 hrs
Orbits/year	100	37.5

Since the dark time to light time ratio is relatively small, the optimum constant power load level for this case can approach the maximum power level available for recharging. With a maximum solar panel output of 50 watts and a charge regulator efficiency of 80 to 90 percent, the power available for recharging the battery will be 40 to 45 watts.

Batteries selected for this application and the conditions under which they must operate are summarized in tables II and III. For Orbit A, cells have been selected on the basis of the discharge current, depth of discharge and operating temperature range. In order to prevent the minimum voltage from falling below 12.0 volts, the plateau

voltage of a silver-cadmium cell under discharge cannot fall below 1.00 volt. As shown in Figure 5-1, at -20°C the discharge rate should not exceed approximately 0.3C. Similarly, in order to prevent the minimum voltage from falling below 12.0 volts, the plateau voltage of a silver-zinc cell, under discharge should not fall below 1.33 volt. Figure 5-2, therefore, shows that at -20°C this type of cell should not be discharged at rates greater than 0.5C. Although smaller cell sizes are possible with proper thermal conditioning of the battery, the cell size selection is also controlled by the permissible depth of discharge. For satisfactory battery performance over a minimum of 100 charge-discharge cycles, the depth of discharge should not exceed 50 percent.

In the case of Orbit B, cell selection has been determined by the power requirements during discharge with the depth of discharge limited to 50 percent or less. The percent of battery capacity as a function of temperature and rate of discharge is shown in Figure 5-3 for a silver-cadmium cell and in Figure 5-4 for a low-rate silver-zinc cell.

For both orbits, the number of cells for each battery system has been defined by the minimum discharge voltage level established for battery operation. In the case of silver-cadmium, a nominal voltage

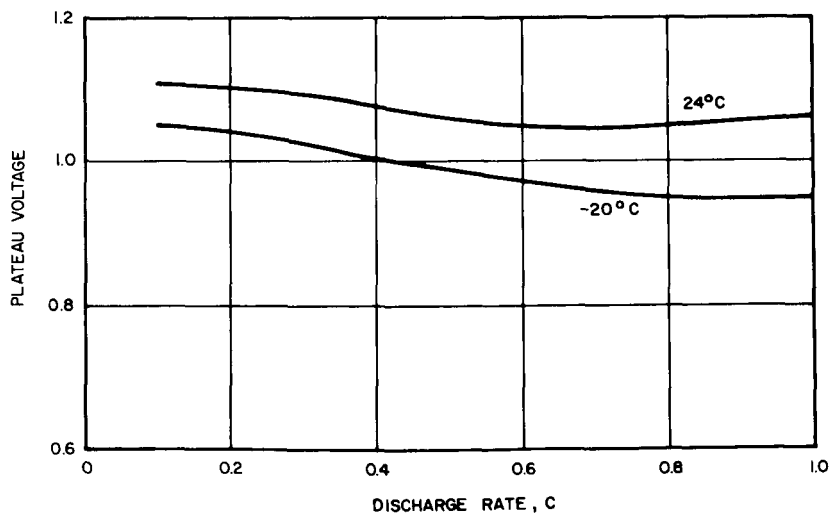

Figure 5-1. Silver-cadmium characteristics.

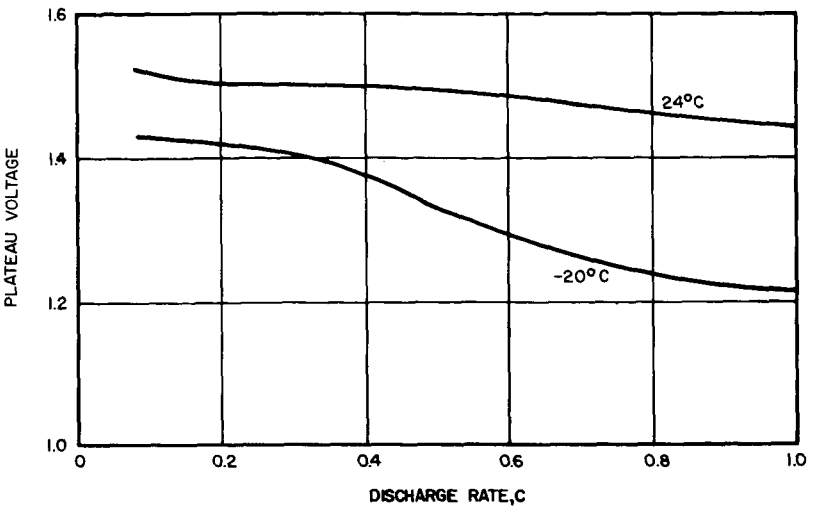

Figure 5-2. Silver-zinc characteristics.

of 1.1 volt per cell was used and in the case of silver-zinc this nominal voltage was 1.5 volts per cell. For the silver-cadmium system, a battery pack of 12 series-connected cells is needed. With the silver-zinc system, the number of cells can be reduced to 9 resulting in an appreciable reduction in battery weight.

It should be noted that although the battery systems for Orbit B weigh six times as much as for Orbit A, approximately thirty times as much power is available during the dark period of Orbit B than during Orbit A. Useable capacities are 0.2 - 0.3 AHR/lb for Orbit A and 1 - 2 AHR/lb for Orbit B.

5.2 CASE II

This involves the use of an oriented solar cell array in a circular earth orbit. Approximately 250 watts of power are available at the solar panel output terminals. Output voltage will range from 25 to 40 volts.

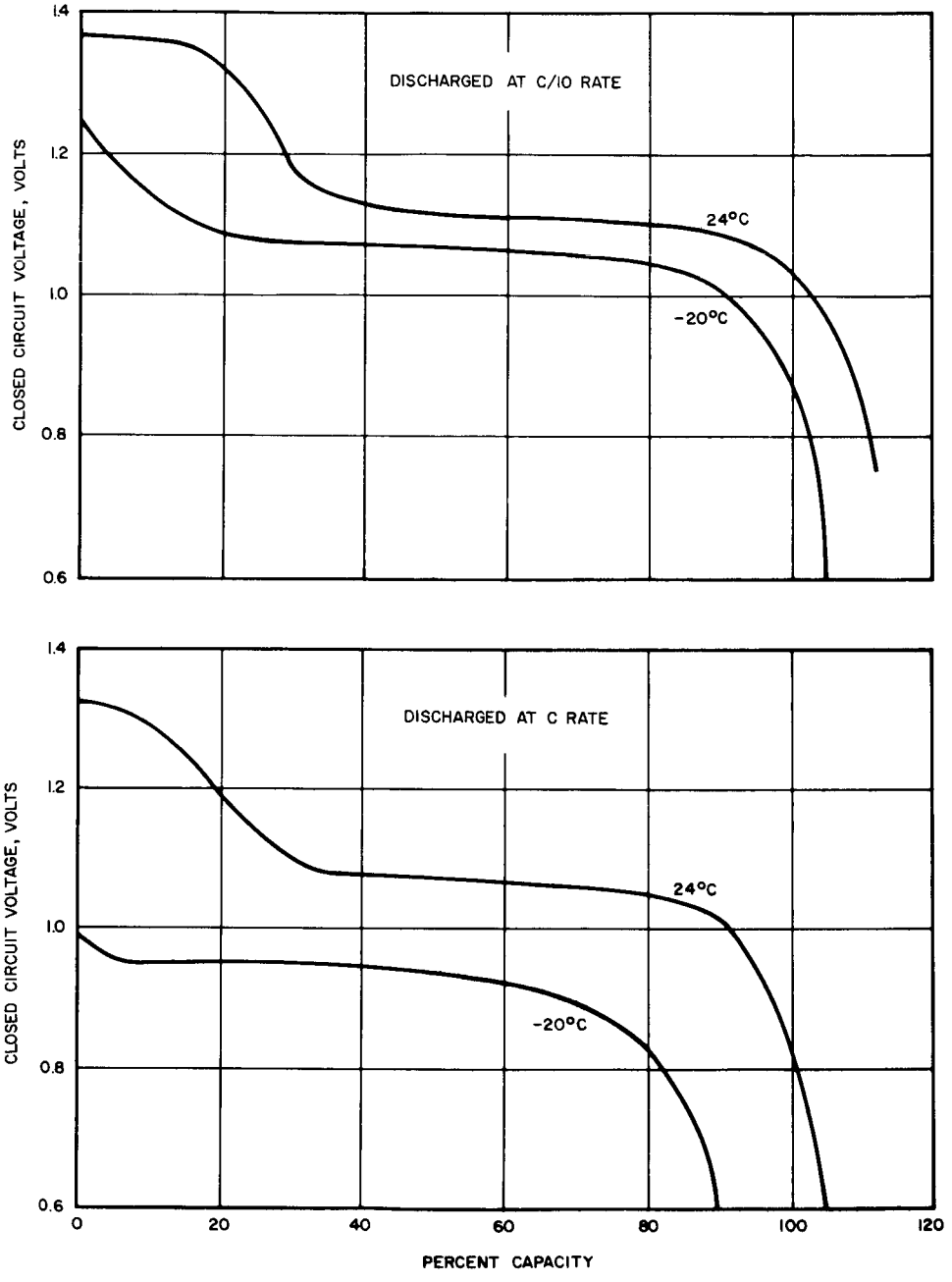

Figure 5-3. Silver-cadmium discharge characteristics.

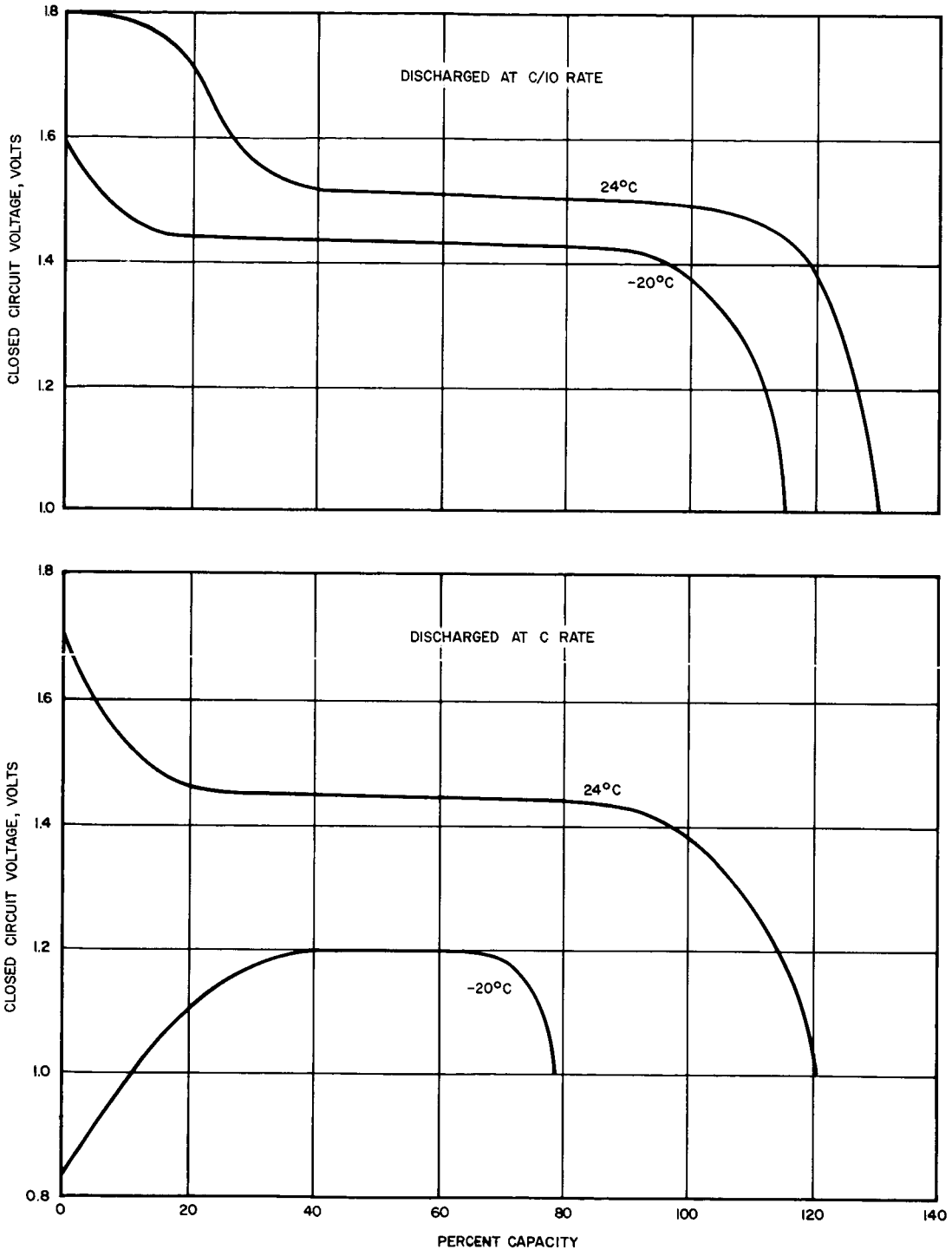

Figure 5-4. Silver-zinc discharge characteristics.

Orbital periods for the circular earth orbit of Case 2 were derived from Figure 5-5 and are summarized as follows:

Orbital Distance	300 miles	600 miles
Orbital Period	1.55 hrs	1.70 hrs
Dark time/orbit	0.59 hrs	0.57 hrs
Charge time/orbit	0.96 hrs	1.13 hrs
Orbits/day	15.5	14.1
Orbits/year	5651	5153

Sealed, sintered-plate, nickel-cadmium cells were selected for this application. The optimum constant power load levels were determined for each orbital distance. These values take into account the fact that due to internal losses, 125 percent of the cell's rated capacity must be recharged in order to return the cell to maximum capacity. With a maximum solar panel output of 250 watts and a charge regulator efficiency of 80 to 90 percent, the power available for recharging will be between 200 and 225 watts.

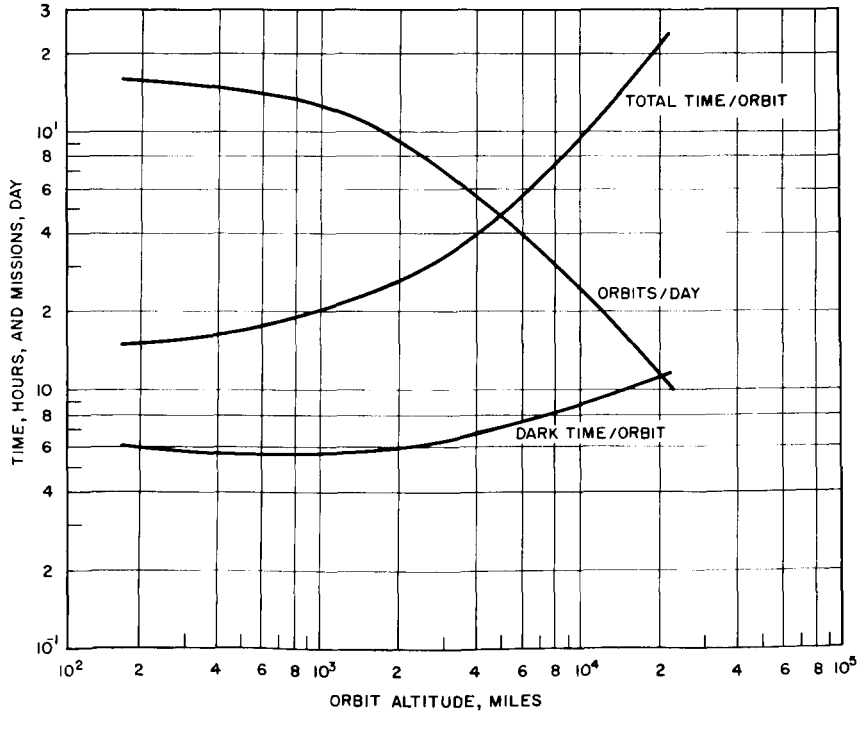

Figure 5-5. Orbital data.

The optimum constant power load levels were determined by consideration of the following factors:

1. The satellite power load levels are identical during the light and dark periods of each orbit.
2. For complete recharge, 125 percent of battery capacity removed must be returned.

The following simplified relationship was derived to enable optimum power levels to be calculated:

$$(W_{OCR} - W_D)\, t_c = 1.25\, W_D t_D$$

where

W_{OCR} = Watts available from optimum charge regulator

W_D = Watts available during charge or discharge

t_c = time for charging, hours

t_D = time for discharge, hours

For the 300 mile orbit, a 200 watt recharge capability would allow a maximum continuous discharge of 113 watts during the entire orbit and assure complete recharge of the battery during the light or recharge period of the orbit. By increasing this recharge capability to 225 watts, the maximum continuous discharge level would be increased to 127 watts. For the 600 mile orbit, 123 watts could be discharged and recharged at 200 watts or 138 watts could be discharged if recharged at the 225 watt level.

The number of cells required for the mission was based on a discharge voltage of 1.2 volts per cell at 70°C and a battery operating voltage range of 25 to 34 volts. A series connected 28 cell nickel-cadmium battery would show 33.6 volts during discharge at 70°C. Under load at -20°C, this battery voltage would be reduced by approximately 0.1 volt per cell to 30.8 volts. Similarly a 22 cell battery would produce 26.4 volts at 70°C and 24.2 volts at -20°C under load.

The size of each battery cell was determined by the optimum charge rate with the depth of discharge limited to 50 percent. For optimum battery performance, the recommended constant current charge rate for conventional sealed, sintered-plate nickel-cadmium cells is C/15. Higher charge rates would produce a build-up of gas pressure within the cell with subsequent rupture and battery failure. Batteries selected for this application and the conditions under which they must operate are summarized in Tables IV and V.

Size "A" corresponds to the conventional cell and its size was determined by multiplying the optimum charge current by 15. This is the minimum cell size for charging at the C/15 rate. Sealed nickel-cadmium cells are also available with a "third electrode" (General Electric) or "adhydrode" (Gulton). This type of cell allows higher charge rates (C/2) without increasing internal cell pressure. Evolved gases are caused to recombine at a rate in equilibrium with the rate of evolution. Size "B" corresponds to this type of cell. Its size was determined by multiplying the charge current by 2. Another method that permits higher charge rates is the "Stabister" system (Sonotone-Mallory). This is a dual diode circuit which diverts excess charge current around fully charged cells. Since a smaller, lighter battery could be used with a minimum loss of time for recharging, these cells should be considered.

Recent conversations with Sonotone have centered around the use of coulometers for measuring battery state-of-charge as well as for limiting overcharge.

5.3 TEMPERATURE EFFECTS

Battery characteristics during charge and discharge are affected by the ambient temperature. A review of recent Crane and Inland Test Laboratories reports (QE/C 65-356 and NAS 5-1048, 1965) leads to the conclusion that both cell capacities and cycle life are detrimentally affected by high temperatures. Figure 5-6 - Battery Capacity vs. Temperature illustrates the fact that temperatures above 25^{o}C immediately reduce the initial capacity of nickel-cadmium cells. A further

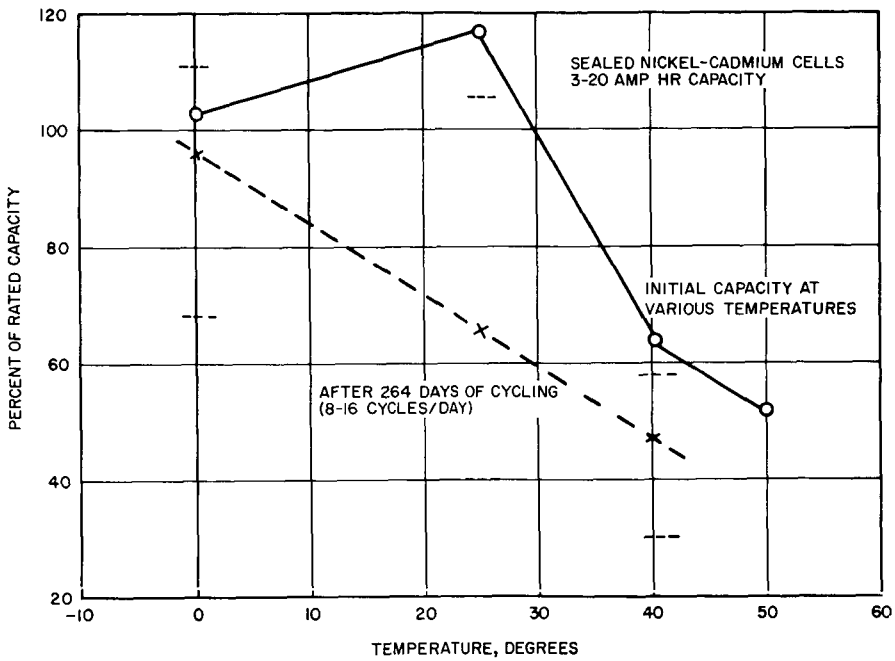

Figure 5-6. Battery capacity vs temperature.

observation is that less than 50 percent of rated capacity remains after 4200 1.5 hour cycles when a temperature of 40°C is used. It is recommended, therefore, that ambient temperatures of nickel-cadmium batteries be confined to the range of -20° to +40°C.

The silver-zinc and silver-cadmium batteries being considered in Case I encounter similar temperature effects. The rate of self discharge must be considered during the long charge period (i.e., 3.5 to 9 days). Storage of batteries at temperatures of 70°C (160°F) results in a capacity loss of 50 percent in two days. A reasonable temperature range for future experiments is -20°C to +40°C. At 40°C, the capacity loss would be 1.0 - 1.5 percent per day.

Cell Type	Cell Capacity amp-hrs	Discharge amp-hrs	% Depth of Discharge	Number of Cells	Battery Weight (Pounds)	OCR Output (Watts)	Charging				Discharging			
							Time (hrs)	Average Watts	Volts	Average * amps	Time (hrs)	Watts	Volts	Amps
AgCd	10	1.45	14.5	12	6.9	40	87	1	19.2	.05	0.5	39	13.2	2.9
AgCd	10	1.65	16.5	12	6.9	45	87	1	19.2	.05	0.5	44	13.2	3.3
AgZn	6	1.40	22.5	9	4.6	40	87	1	18.5	.05	0.5	39	13.5	2.8
AgZn	6	1.60	27.	9	4.6	45	87	1	18.5	.05	0.5	44	13.5	3.2

Table I. Case I, orbit A, (100 cycles/year)

Cell Type	Cell Capacity amp-hrs	Discharge amp-hrs	% Depth of Discharge	Number of Cells	Battery Weight (Pounds)	OCR Output (Watts)	Charging				Discharging			
							Time (hrs)	Average Watts	Volts	Average * amps	Time (hrs)	Watts	Volts	Amps
AgCd	100	43.2	43	12	41	40	218	4	19.2	.20	16	36	13.2	2.7
AgCd	100	49.6	50	12	41	45	218	4	19.2	.20	16	41	13.2	3.1
AgZn	100	41.6	42	9	25	40	218	4	18.5	.21	16	36	13.5	2.6
AgZn	100	48.0	48	9	25	45	218	4	18.5	.21	16	41	13.5	3.0

*Maximum charge rate will be approximately 1.0 Amp and will be reduced to 0.1 Amps when battery end-of-charge voltage has been reached.

Table II. Case I, orbit B, (38 cycles/year)

Number of Cells	OCR Output (watts)	Charging				Discharging			
		Time (hrs)	Watts	Volts	Amps	Time (hrs)	Watts	Volts	Amps
22	200	0.96	87	31.5	2.76	0.59	113	26.4	4.25
22	225	0.96	98	31.5	3.11	0.59	127	26.4	4.80
28	200	0.96	87	40.0	2.17	0.59	113	33.6	3.36
28	225	0.96	98	40.0	2.45	0.59	127	33.6	3.80

		Cell Size "A"				Cell Size "B"			
Number of Cells	OCR Output (watts)	Capacity amp-hrs	% Depth of Discharge	Discharge amp-hrs	Battery wt. (pounds)	Capacity amp-hrs	% Depth of Discharge	Discharge amp-hrs	Battery wt. (pounds)
22	200	41	5	2.50	105	6.5	39	2.50	14.3
22	225	46	5	2.83	121	7.4	39	2.83	16.3
28	200	32	5	1.98	109	5.2	38	1.98	14.5
28	225	37	5	2.25	123	5.8	39	2.25	15.2

Table III. Case 2, 300 mile orbit

Number of Cells	OCR Output (watts)	Charging				Discharging			
		Time (hrs)	Watts	Volts	Amps	Time (hrs)	Watts	Volts	Amps
22	200	1.13	77	31.5	2.44	0.57	123	26.4	4.64
22	225	1.13	87	31.5	2.76	0.57	138	26.4	5.20
28	200	1.13	77	40.0	1.92	0.57	123	33.6	3.67
28	225	1.13	87	40.0	2.17	0.57	138	33.6	4.11

		Cell Size "A"				Cell Size "B"			
Number of Cells	OCR Output (watts)	Capacity amp-hrs	% Depth of Discharge	Discharge amp-hrs	Battery wt. (pounds)	Capacity amp-hrs	% Depth of Discharge	Discharge amp-hrs	Battery wt. (pounds)
22	200	36	6	2.65	97	5.8	46	2.65	12.8
22	225	41	6	2.95	105	6.5	46	2.95	14.3
28	200	28	6	2.10	95	4.6	46	2.10	12.8
28	225	32	6	2.34	109	5.2	45	2.34	14.5

Table IV. Case 2, 600 mile orbit

Figures 5-7 and 5-8 provide solar cell array electrical characteristic curves and their variation with temperature for the two cases.

Case 1 is a spin stabilized array providing 50 watts at 30°C under normally incident solar illumination. For a normally illuminated paddle to provide 50 watts, it would typically consist of a solar cell matrix of 56 cells in series and 34 cells in parallel. The 50 watts is treated as an initial requirement; accounting for radiation damage would require a larger array and would depend on type of cell coverglass, orbit, lifetime, and solar flare activity. The rotation of the solar paddles in Case 1 and the resultant shadowing can be expected to cause power excursions of -30 percent.

Case 2 is an oriented solar cell array providing 250 watts at 30°C. Assuming the array is planar, it would consist of a solar cell matrix of 93 in series by 105 in parallel with equipotential points connected in parallel. Degradation caused by Van Allen and/or solar flare particulate radiation has not been taken into account.

The characteristic curves provided for Cases 1 and 2 are based on arrays assembled with N on P, 10 ohm-centimeter, 1 x 2 centimeter solar cells. Cell space efficiency is approximately 10.2 percent. Normally, such arrays would be divided into diode isolated sections to enhance reliability. Diode drops have not been shown in the characteristic curves and would alter the curve shapes near the open circuit voltage.

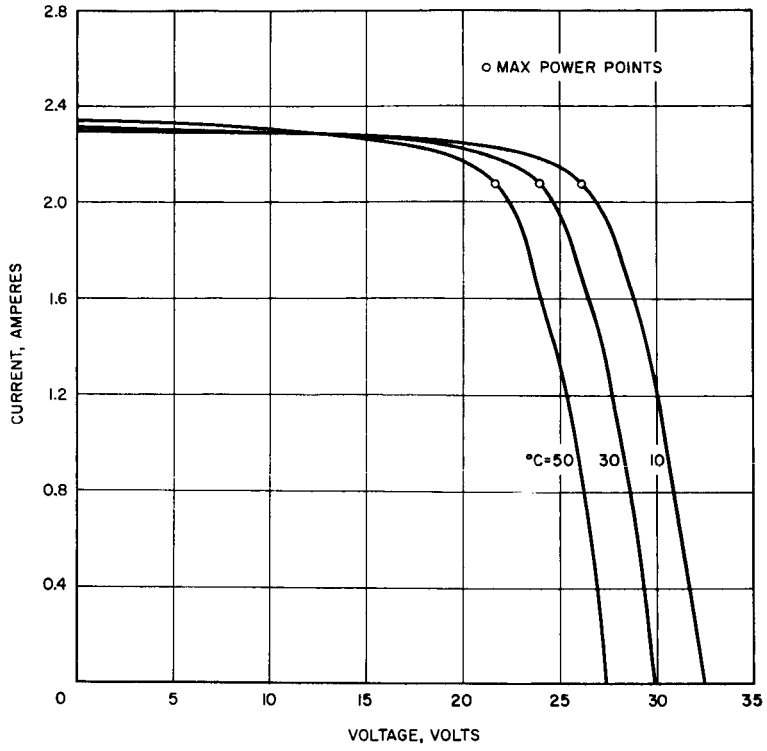

Figure 5-7. Characteristic curves of solar array providing 50 watts maximum at 30°C (N/P cells).

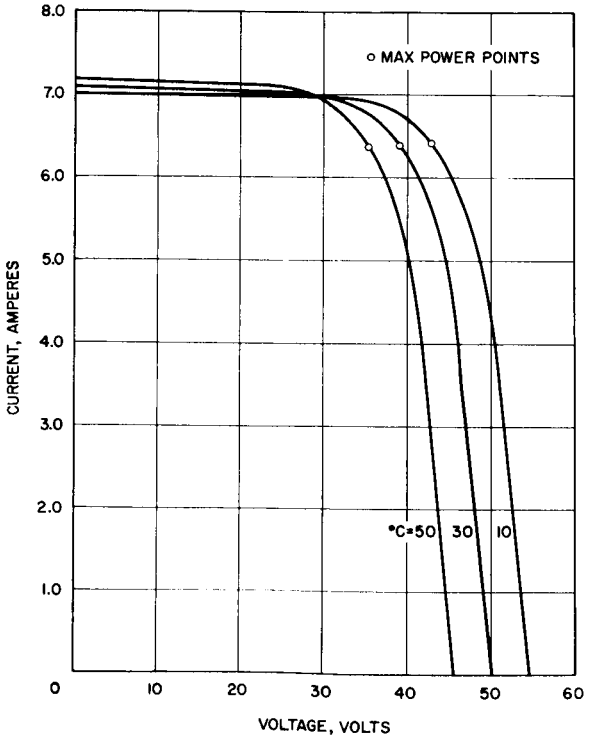

Figure 5-8. Characteristic curves of solar array providing 250 watts maximum at 30°C (N/P cells).